EK-DLV1J-UG-001

DLV11-J user's guide

digital

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EK-DLV1J-UG-001

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CHAPTER 1
INTRODUCTION

1.1 INTRODUCTION

This manual contains all user information required for installing, interfacing, and programming the DLV11-J 4-Channel Asynchronous Serial Line Unit (SLU) Interface.

The DLV11-J is an LSI-11 bus-compatible interface module (M8043) that contains four asynchronous serial line channels. Serial line channels can be independently configured for Electronics Industry Association (EIA) RS-422, RS-423, or RS-232C signal compatibility. Provisions are also made for configuring the channels for 20 mA current loop (and "reader run") via the DLV11-KA 20 mA option (described in Appendix A). Each DLV11-J module has the following features:

- Four independent serial line interfaces exist with consecutive bus device address and vector assignments that can be user-configured for system requirements.

- Each channel can be independently configured for any of the following selections.

  Crystal-Controlled Baud Rates – 150, 300, 600, 1200, 2400, 4800, 9600, 19200, or 38400 bits per second (bits/s) – 110 bits/s is available when the DLV11-KA option is installed.

  Number of Data Bits - 7 or 8.

  Number of Stop Bits - 1 or 2.

  Parity Bit - No parity or parity; and even or odd parity.

- One channel (channel 3) can be designated the console device. In most configurations, each LSI-11 system requires one keyboard/display terminal that will function as the console device.

- All data buffers (one transmit and one receive) in each channel are double-buffered.

- Channel 3 can be configured to respond to a receive line BREAK condition by causing the processor to either halt (console emulator mode), bootstrap the system, or have no response.

- The module has on-board overload protection (fuse) for 20 mA (current loop power source to DLV11-KA option).

- The DLV11-J is completely LSI-11 bus-compatible, and will function in all present LSI-11 systems.

1.2 SPECIFICATIONS

1.2.1 Electrical

M8043 Module Power Requirements
+5 V ±5%, 1 A typical (1.25 A max.)
+12 V ±3%, 0.15 A typical (0.2 A max.)
Note: Add 0.225 A for each DLV11-KA option installed.

Bus Loading
ac loading = 1 unit load
dc loading = 1 unit load

Interface Connector Pinning
Four 10-pin connectors (one for each channel) are provided on the DLV11-J module. Connector pins and signal functions are described in Figure 1-1 and Table 1-1.

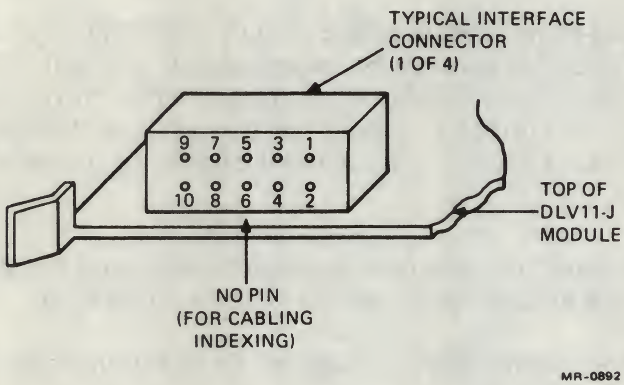

Figure 1-1 DLV11-J Connector Pinning

Table 1-1 DLV11-J Connector Pinning Description

Pin	Signal/Function
1	UART CLK (16 × baud rate, C MOS Levels)
2	Signal Ground
3	Transmitted Data (EIA RS-232C, RS-423 and 20 mA); Transmitted Data (+) (EIA RS-422)
4	Signal Ground (EIA RS-232C and RS-423); Transmitted Data (-) (EIA RS-422), RDR Run Pulse (20 mA)
5	Signal Ground
6	Indexing Key (no pin)
7	Received Data (-)
8	Received Data (+)
9	Signal Ground
10	Fused +12 V

Interface Signal Level
Factory Configuration: All channels are configured to meet both EIA RS-423 and RS-232C signal compatibility simultaneously.

Optional Configurations: Channels can be user-configured for EIA RS-422 or 20 mA current loop (20 mA current loop operation requires the use of the DLV11-KA 20 mA current loop option).

1.2.2 Environmental

Operating: 5° to 60° C (41° to 140° F) with a relative humidity of 5% to 95% (noncondensing), with adequate airflow across the module. When operating at the maximum temperature (60° C or 140° F), air flow must maintain the inlet-to-outlet air temperature rise across the module at not more than 5° C (9° F).

Storage: -40° to 80° C (-40° to 176° F) with a relative humidity of 5% to 95% (noncondensing).

NOTE
Before operating a module that has been stored in an environment outside the specified operating environment, the module must be allowed to stabilize at the operating temperature for 5 minutes (minimum).

1.2.3 Physical

Height	13.2 cm (5.2 in) typical
Width	1.27 cm (0.5 in) typical
Length	22.8 cm (8.9 in) typical

NOTE
Length as stated is approximate and includes plastic handles. Actual module length is 21.6 cm (8.5 in).

Weight 0.23 kg (8 oz) typical

1.2.4 Module Contact Finger Identification
The DIGITAL finger (pin) identification for dual-height boards is shown in Figure 1-2.

1.2.5 Backplane Pinning Utilization
DLV11-J backplane pin utilization is shown in Table 1-2. Blank spaces indicate pins not used.

1.3 OPTIONS

1.3.1 Cables
The DLV11-J may work in conjunction with several peripheral device cables and options, thus providing great flexibility when configuring systems. Figure 1-3 shows the possible cables and options used with the DLV11-J as well as the primary application of each.

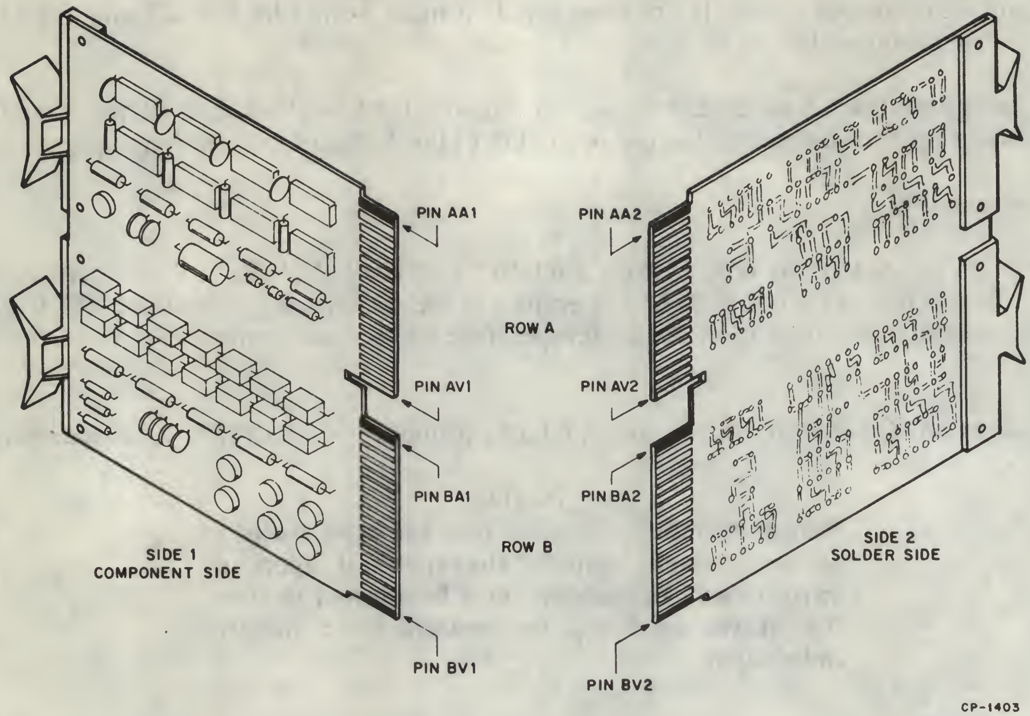

Figure 1-2 Module Contact Finger Identification

Table 1-2 Backplane Pin Utilization

A Connector			B Connector		
Side 1	**Pin**	**Side 2**	**Side 1**	**Pin**	**Side 2**
	A	+5 V	BDCOK H	A	+5 V
	B			B	
	C	GND		C	GND
	D	+12 V		D	
	E	BDOUT L		E	BDAL2 L
	F	BRPLY L		F	BDAL3 L
	H	BDIN L		H	BDAL4 L
GND	J	BSYNC L	GND	J	BDAL5 L
	K			K	BDAL6 L
	L	BIRQ L		L	BDAL7 L
GND	M	BIAKI L	GND	M	BDAL8 L
	N	BIAKO L		N	BDAL9 L
BHALT L	P	BBS7 L		P	BDAL10 L
	R	BDMGI L		R	BDAL11 L
	S	BDMGO L		S	BDAL12 L
GND	T	BINIT L	GND	T	BDAL13 L
	U	BDAL0 L		U	BDAL14 L
	V	BDAL1 L	+5 V	V	BDAL15 L

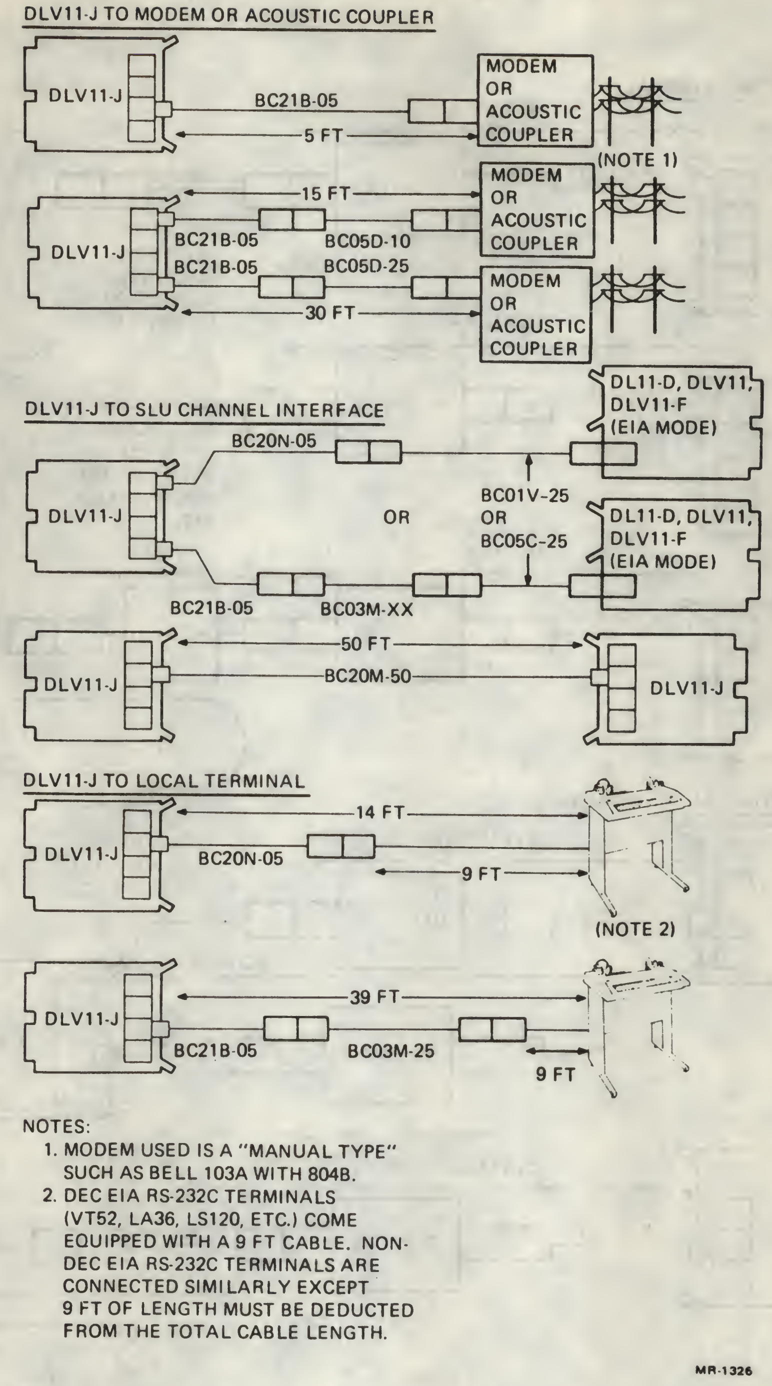

Figure 1-3 DLV11-J Cabling Summary

1.3.2 DLV11-KA 20 mA Current Loop Option

The DLV11-J module has the ability to interface with 20 mA current loop devices including those with "reader-run" capabilities. This is accomplished with the use of the DLV11-KA option. The option consists of a DLV11-KB (EIA to 20 mA current loop converter) and a BC21A-03 interface cable. The DLV11-KA is placed between the DLV11-J module output and the 20 mA current loop peripheral device. Figure 1-4 illustrates the cables and devices which may be used with the DLV11-KA option. For detailed information on the DLV11-KA option see Appendix A.

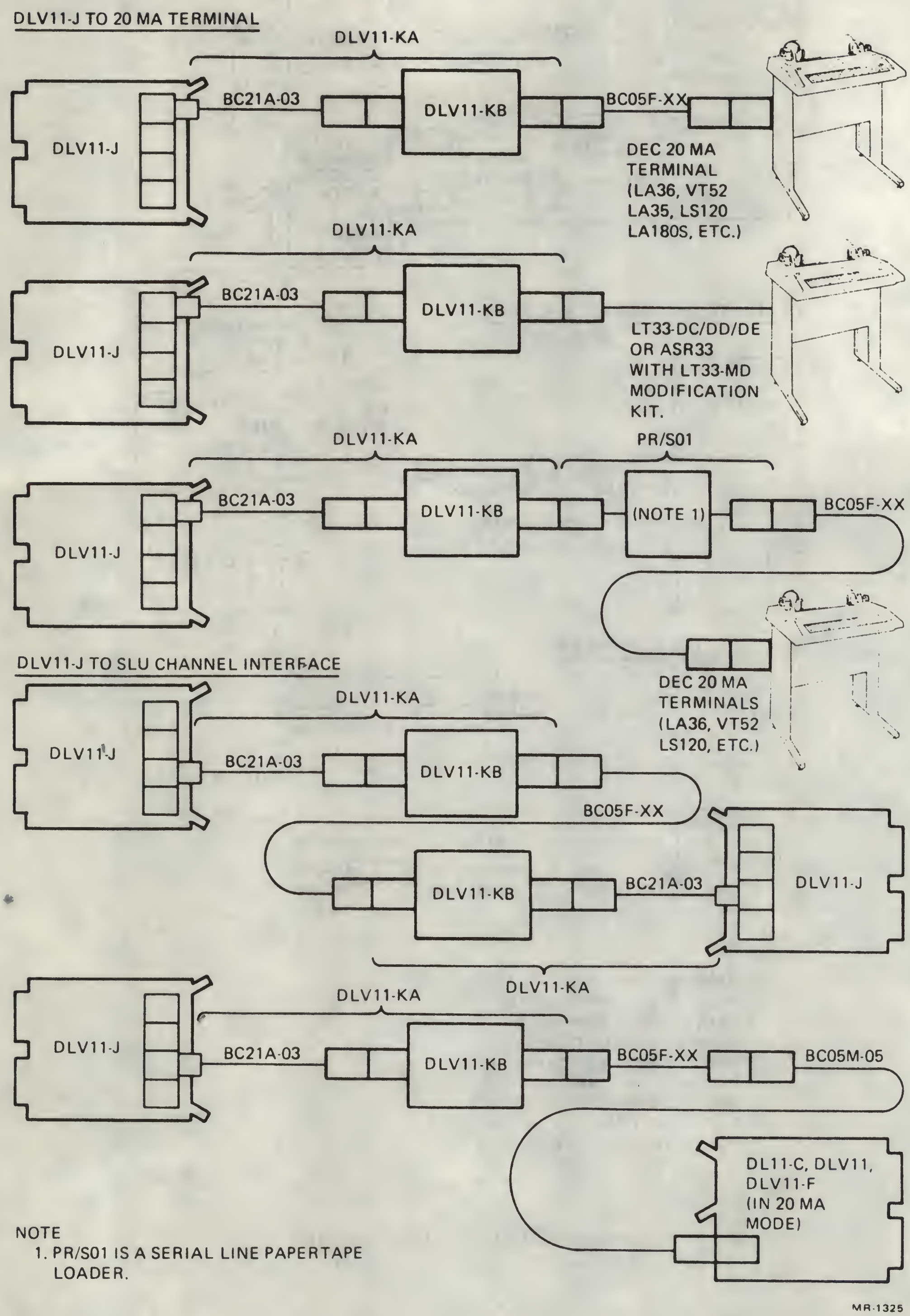

Figure 1-4 DLV11-J 20 mA Cabling Summary

CHAPTER 2
INSTALLATION

2.1 INTRODUCTION

The DLV11-J can be installed in any system that uses an LSI-11 bus structure. This includes LSI-11 and LSI-11/2 component systems, PDP-11/03, PDP-11V03, and PDP-11T03 systems.

Installation involves the following steps.

1. Jumpers on the DLV11-J module are configured for the specific mode of operation required by the user.

2. The module is installed in the LSI-11 system backplane.

3. Up to four peripherals (terminals, printers, etc.) can be connected to the DLV11-J module.

The DLV11-J is factory-configured for the following operation.

- Base Device Register Address = 176500

- Base Vector = 300

- Channel 3 enabled as the console device (device register addresses 177560-177566 and vectors = 60 and 64)

- Channel 3 Halt on BREAK enabled

- Baud rates (transmit and receive are identical):

  Channels 0, 1 and 2 = 9.6K bits/s

  Channel 3 = 300 bits/s

- Data/parity/stop bit format (all channels):

  Number of data bits = 8

  Number of stop bits = 1

  Parity = parity disabled

- Serial line signal interface levels (all channels) meet both Electronics Industry Association (EIA) RS-232C and RS-423 signal levels, simultaneously (slew rate = 2 μs)

Figure 2-1 gives the location of components and jumpers used to configure the DLV11-J module to meet user requirements. Table 2-1 gives a summary of the factory configuration of these components and jumpers with a brief explanation of their purpose.

The remainder of this chapter contains specific instructions for configuring and installing the DLV11-J.

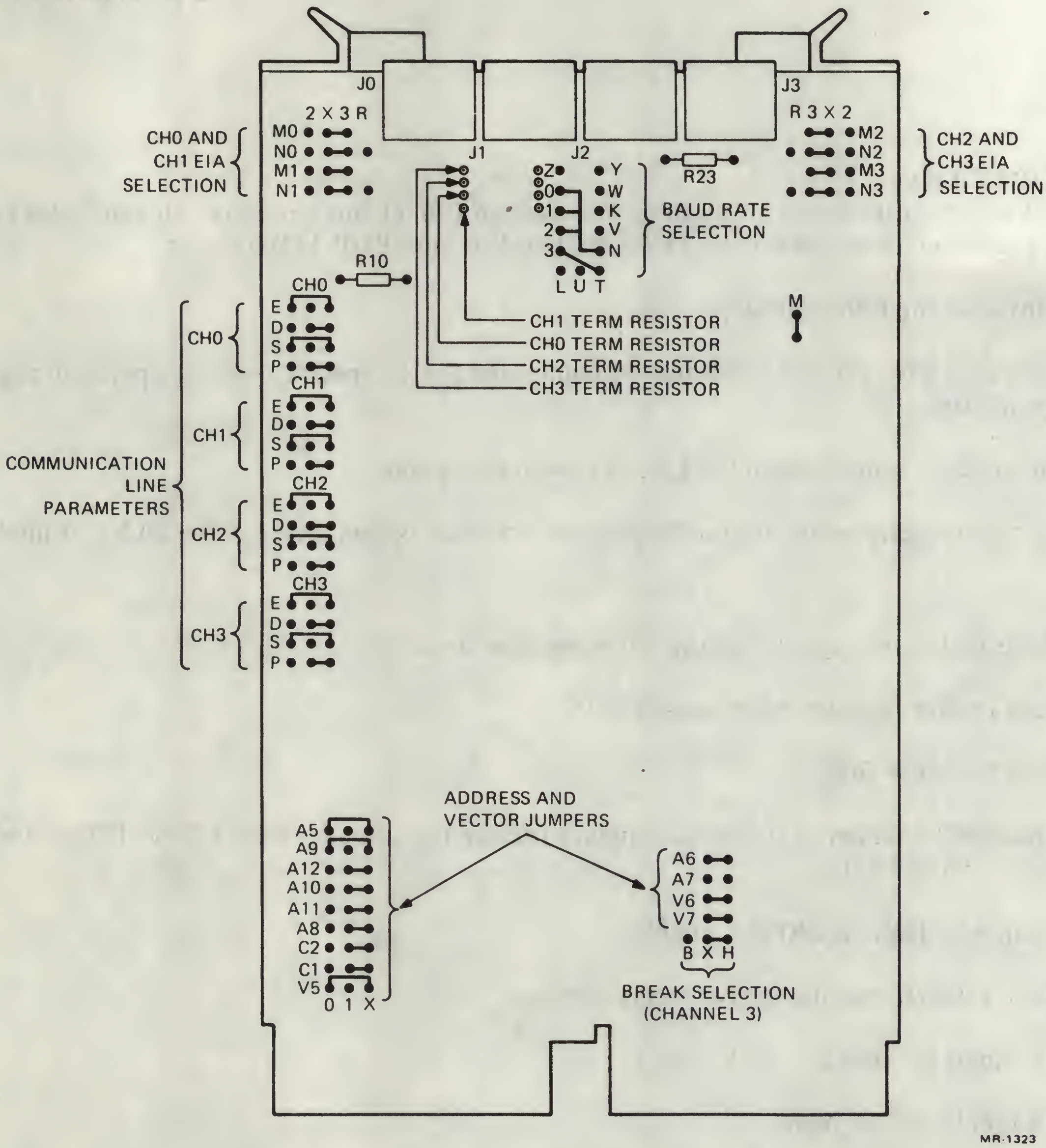

Figure 2-1 DLV11-J Component and Jumper Factory Configuration Summary

Table 2-1 DLV11-J Component and Jumper Factory Configuration Summary

Label	Configuration	Function Implemented
A12 A11 A10 A9 A8 A7 A6 A5	X to 1 X to 1 X to 1 X to 0 X to 1 R* I* X to 0	This arrangement of jumpers A5–A12 implements the octal base device address 1765XX, which is the assigned address for channel 0 RCSR. The least significant digit is decoded on the module during operation to address one of four SLU device registers as follows. LSD = 0 = RCSR LSD = 2 = RBUF LSD = 4 = XCSR LSD = 6 = XBUF
C1 C2	X to 1 X to 1	These jumpers are used to enable channel 3 for console operation. Base address must be 176500 (factory-configured), 176540 or 177500.
BREAK Response	X to H	This jumper determines channel 3 BREAK response. The board is configured for halt (console emulator mode) upon receiving a BREAK condition).
V7 V6 V5	I* I* X to 0	This arrangement of jumpers V5–V7 implements the octal base vector of 300 with channel 3 at 60 and 64.
E D S P	X to 0 X to 1 X to 0 X to 1	Odd parity enabled 8 data bits 1 stop bit No parity These jumpers determine the word format used by the channel. All channels are configured the same at the factory.
0 1 2 3	0 to N 1 to N 2 to N 3 to T	9.6K baud 9.6K baud 9.6K baud 300 baud These jumpers determine the baud rate (bits/s) of the serial line channel. If more than one channel requires the same baud rate, daisy-chain the wirewrap pins.
M	I*	Always installed, removed only during production test.
N0–N3 M0–M3	X to 3 X to 3	These jumpers determine the EIA standard compatibility of the channels. All channels are set at the factory to be compatible to both EIA RS-423 and RS-232C simultaneously.
R10	22K ohms	Channels 0 and 1 slew rate of 2 μs (used when configured for EIA RS-423/RS-232C)
R23	22K ohms	Channels 2 and 3, slew rate of 2 μs (used when configured for EIA RS-423/RS-232C)

*R = jumper removed; I = jumper installed

2.2 CONFIGURING MODULE JUMPERS

2.2.1 General

The DLV11-J device register addresses, interrupt vectors, serial word formats, baud rates, etc., are selected by installing and/or removing jumpers. Wirewrap posts are provided on the module for this purpose. The module is factory-configured and ready for use in many user applications. However, as your system applications require different DLV11-J device register addresses and interrupt vectors and/or operations, refer to appropriate paragraphs for configuration instructions.

2.2.2 Addressing

2.2.2.1 Device Register Addresses – The DLV11-J module contains 16 device registers that can be individually addressed by the computer program. Four device registers (RCSR, RBUF, XCSR and XBUF) are provided for each of the four serial line channels (channels 0–3). Jumpers are configured to establish a base device register address (BA) for the module. This base device address is the address of the channel 0 received control/status register (RCSR). The format of a device address is shown in Figure 2-2. The location of the jumpered wirewrap posts used to configure the base device address can be seen in Figure 2-3. Note that address bits 13–17 are neither configured on nor decoded by the DLV11-J module. These bits are decoded by the processor module as the bank 7 select (BBS7 L) bus signal. This signal becomes active only when the upper 4K address space is accessed. Bits 3–4 are not user-configured; they select the serial line channel to be used within the module. Similarly, address bits 1–2 select one of the four device registers within the addressed channel.

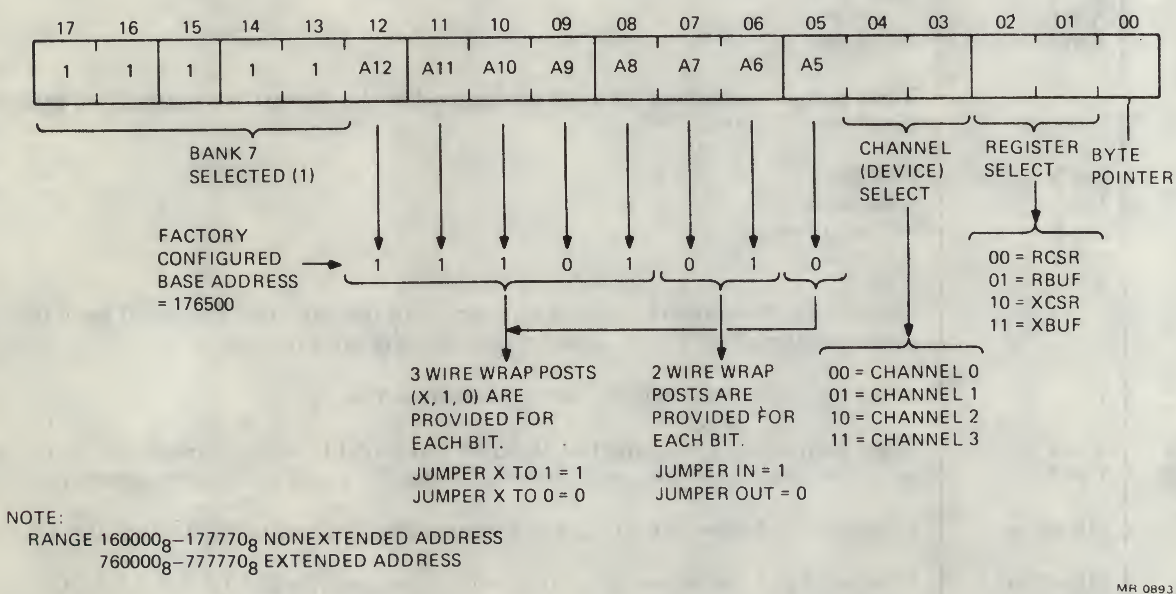

Figure 2-2 Device Register Address Format

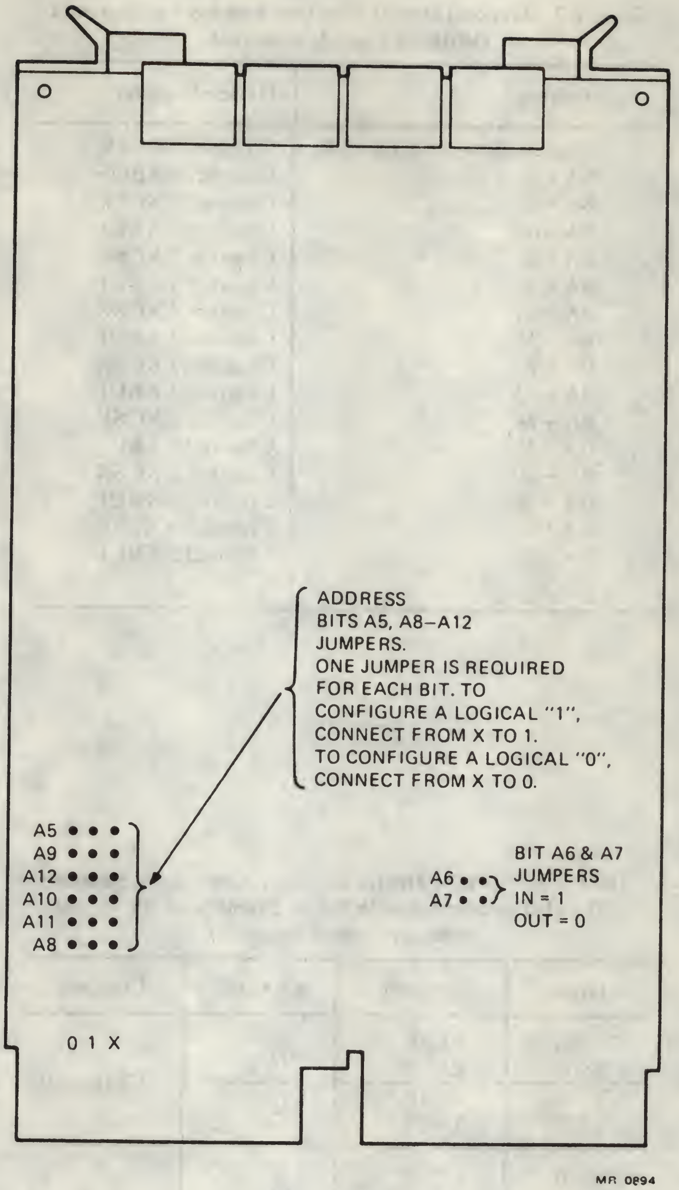

Figure 2-3 Device Register Address Jumper Locations

The device addresses of the module follow the configured base device address (BA) consecutively through 16 (total) contiguous word addresses. Each device address is an offset of the base device address as shown in Table 2-2. Table 2–3 gives a numerical example of the device addresses of the DLV11-J when a base device register address of 176500 and base interrupt vector of 300 are configured. (Base interrupt vectors are described in Paragraph 2.2.2.2.)

It is possible to independently configure the last four addresses (channel 3) to the LSI-11 console device (addresses 177560–177566) when certain base addresses and console select jumpers are installed. In this configuration, the preceding addresses (channels 0, 1 and 2) are not affected; they are normal offsets of the configured base device address as shown in Table 2-4.

Table 2-2 General Device Register Address Assignments (Without console selected)

Address	Device Register
Module Base Address (BA)	Channel 0 RCSR
BA + 2	Channel 0 RBUF
BA + 4	Channel 0 XCSR
BA + 6	Channel 0 XBUF
BA + 10	Channel 1 RCSR
BA + 12	Channel 1 RBUF
BA + 14	Channel 1 XCSR
BA + 16	Channel 1 XBUF
BA + 20	Channel 2 RCSR
BA + 22	Channel 2 RBUF
BA + 24	Channel 2 XCSR
BA + 26	Channel 2 XBUF
BA + 30	Channel 3 RCSR
BA + 32	Channel 3 RBUF
BA + 34	Channel 3 XCSR
BA + 36	Channel 3 XBUF

Table 2-3 Specific Device Register Address Assignments (DLV11-J configured with BA = 176500 and BV = 300 without console selected)

Address	Register	Vector	Channel
176500	RCSR	300	Channel 0
176502	RBUF		
176504	XCSR	304	
176506	XBUF		
176510	RCSR	310	Channel 1
176512	RBUF		
176514	XCSR	314	
176516	XBUF		
176520	RCSR	320	Channel 2
176522	RBUF		
176524	XCSR	324	
176526	XBUF		
176530	RCSR	330	Channel 3
176532	RBUF		
176534	XCSR	334	
176536	XBUF		

NOTE
All addresses are in octal notation.

Table 2-4 General Device Register Address Assignments (General configuration with console selected)

Address	Device Register
Module Base Address (BA)	Channel 0 RCSR
BA + 2	Channel 0 RBUF
BA + 4	Channel 0 XCSR
BA + 6	Channel 0 XBUF
BA + 10	Channel 1 RCSR
BA + 12	Channel 1 RBUF
BA + 14	Channel 1 XCSR
BA + 16	Channel 1 XBUF
BA + 20	Channel 2 RCSR
BA + 22	Channel 2 RBUF
BA + 24	Channel 2 XCSR
BA + 26	Channel 2 XBUF
177560	Channel 3* RCSR
177562	Channel 3 RBUF
177564	Channel 3 XCSR
177566	Channel 3 XBUF

*Channel 3 is enabled as a console device.

NOTE
All addresses in octal notation.

The factory-assigned base device register address is 176500 and base vector is 300, producing the individual device register addresses shown in Table 2-5; in addition, channel 3 is enabled as the console device. Configure any base address desired for specific system requirements by installing or removing appropriate wirewrap jumpers. However, if channel 3 is to function as the console device, the base address must be configured for one of three addresses: 176500 (factory configuration), 176540 or 177500.

Table 2-5 Specific Device Register Address Assignments (Factory configuration with BA = 176500, BV = 300 and console enabled)

Address	Register	Vector	Channel
176500	RCSR	300	Channel 0
176502	RBUF		
176504	XCSR	304	
176506	XBUF		
176510	RCSR	310	Channel 1
176512	RBUF		
176514	XCSR	314	
176516	XBUF		
176520	RCSR	320	Channel 2
176522	RBUF		
176524	XCSR	324	
176526	XBUF		
177560	RCSR	60	Channel 3
177562	RBUF		
177564	XCSR	64	
177566	XBUF		

NOTE
All addresses are in octal notation.

Three wirewrap posts each are provided for address bits A8–A12 and A5. One jumper must be installed for each of these bits. Connect the jumper from wirewrap post X (for a particular bit) to a corresponding post labeled 1 or 0 to select the desired address configuration. Address bits A7 and A6 use only two wirewrap posts each; configure each of these bits to logical 1 by installing a jumper, or to logical 0 by removing a jumper.

2.2.2.2 Interrupt Vectors – Two interrupt vectors (one for receive and one for transmit) are provided for each of the four SLU channels (8 vectors total). The interrupt vector format is shown in Figure 2-4. Figure 2-5 illustrates the jumper wirewrap post locations used when configuring the base interrupt vector. The procedure for configuring the vectors is similar to that used for the device register addresses; a base vector is configured on the module with all other vectors being standard offsets from the base vector as shown in Table 2-6. The base vector (BV) is the channel 0 receive interrupt vector of the module. Each interrupt vector references two word locations in memory. Hence, sequential vectors follow the base vector in octal increments of 4 as shown in Table 2-7.

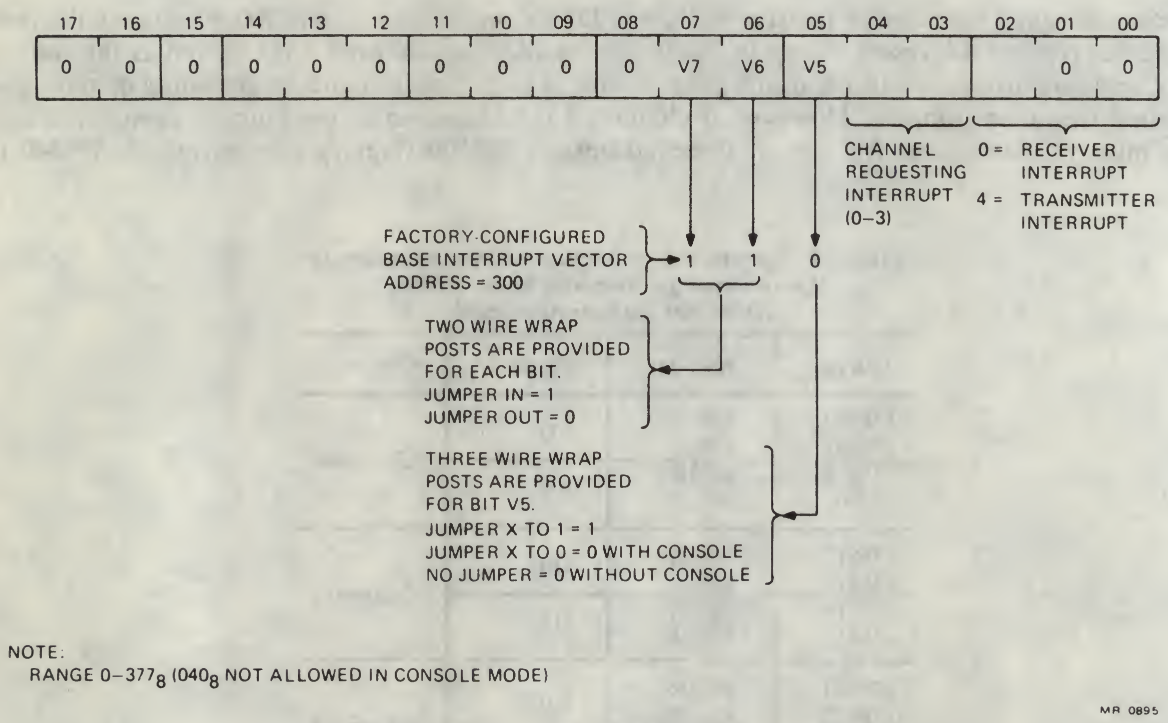

Figure 2-4 Interrupt Vector Format

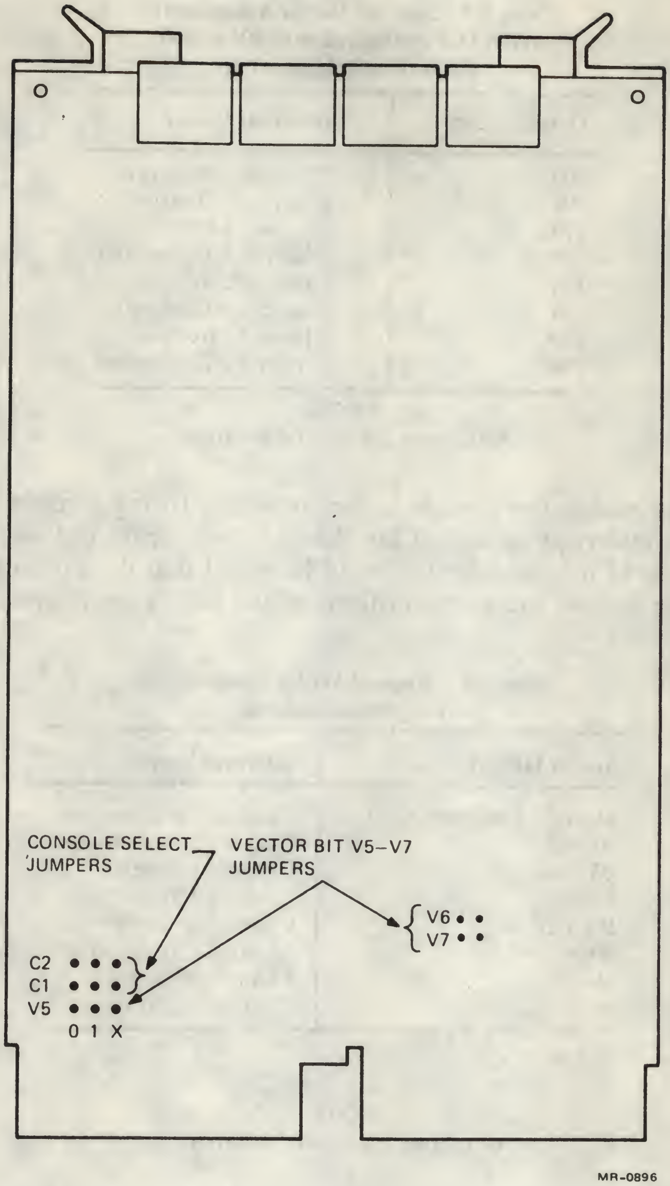

Figure 2-5 Interrupt Vector Address and Console Select Jumper Locations

Table 2-6 General Vector Assignments (Without console selected)

Vector Offsets	Interrupt Vector
Module Base Vector (BV)	Channel 0 Receiver
BV + 4	Channel 0 Transmitter
BV + 10	Channel 1 Receiver
BV + 14	Channel 1 Transmitter
BV + 20	Channel 2 Receiver
BV + 24	Channel 2 Transmitter
BV + 30	Channel 3 Receiver
BV + 34	Channel 3 Transmitter

Table 2-7 Specific Vector Assignments (DLV11-J configured with BV = 300 without console selected)

Octal Vector	Interrupt Vector
300	Channel 0 Receiver
304	Channel 0 Transmitter
310	Channel 1 Receiver
314	Channel 1 Transmitter
320	Channel 2 Receiver
324	Channel 2 Transmitter
330	Channel 3 Receiver
334	Channel 3 Transmitter

NOTE
All vectors are in octal notation.

When channel 3 is configured as the console device interface (using console select jumpers discussed in Paragraph 2.2.2.3) the interrupt vectors of the channel become 60 and 64. This is true regardless of the configured base vector of the module. It should be noted that the preceding channels (0, 1 and 2) are not affected and their vectors are normal offsets of the base vector configured, as shown in Table 2-8.

Table 2-8 General Vector Assignments (With console selected)

Vector Offsets	Interrupt Vector
Module Base Vector (BV)	Channel 0 Receiver
BV + 4	Channel 0 Transmitter
BV + 10	Channel 1 Receiver
BV + 14	Channel 1 Transmitter
BV + 20	Channel 2 Receiver
BV + 24	Channel 2 Transmitter
60	Channel 3 Receiver*
64	Channel 3 Transmitter*

*Console selected

NOTE
All vectors are in octal notation.

The module is factory-configured with a base interrupt vector of 300 and channel 3 is configured as the console device. Therefore, channel 3's interrupt vectors will automatically be 60 and 64, as shown on Table 2-9. When channel 3 is not configured as the console device, channel 3 receiver and transmitter interrupt vectors are equal to the base vector address plus 30 and 34, respectively.

Table 2-9 Specific Vector Assignments (Factory-configured with BV = 300 with console selected)

Octal Vector	Interrupt Vector
300	Channel 0 Receiver
304	Channel 0 Transmitter
310	Channel 1 Receiver
314	Channel 1 Transmitter
320	Channel 2 Receiver
324	Channel 2 Transmitter
60	Channel 3 Receiver*
64	Channel 3 Transmitter*

*Console selected

NOTE
All vectors are in octal notation.

Three wirewrap posts are provided for configuring vector bit V5. To obtain a logical 1 a jumper is installed between wirewrap posts X and 1. Configure a logical 0 with channel 3 not configured as a console device by connecting no jumpers; and to configure a logical zero with channel 3 used as a console device, connect a jumper between the X and 0 wirewrap posts. Two wirewrap posts each are provided for configuring vector bits V6 and V7. To configure a logical 1 for these bits, install jumper(s); to configure a logical 0, remove jumper(s).

A summary of possible vector jumper configurations is given in Table 2-10.

Table 2-10 Summary of Vector Jumper Configurations

Label	Logical 1	Logical 0
V7	Jumper installed	Jumper removed
V6	Jumper installed	Jumper removed
V5	Jumper installed from wirewrap post X to 1	Console not selected – jumper removed
		Console selected – jumper installed from wirewrap post X to 0

2.2.2.3 Console Device Jumpers – When the DLV11-J is used as the LSI-11 console device interface, the module's base device register address must be configured to one of three addresses (176500, 176540 or 177500). In addition, both console device jumpers C1 and C2 whose locations are shown in Figure 2-5 must be connected from their respective X to 1 wirewrap posts. This enables console device address and interrupt vector assignments of the SLU channel 3 as follows.

Device Register Address	Console Device Register	Function	Interrupt Vector
177560	RCSR	Receiver control/status register	60
177562	RBUF	Receiver data buffer register	
177564	XCSR	Transmitter control/status register	64
177566	XBUF	Transmitter data buffer register	

When channel 3 is used as a console device interface, the remaining channels (0, 1 and 2) are not affected. The device register addresses and interrupt vectors associated with these channels are normal consecutive offsets from the module's base configurations.

If console operation is not desired, both console device jumpers C1 and C2 must be connected from their respective X to 0 wirewrap posts. Channel 3's interrupt vectors will then be normal offsets from the module's base vector.

A summary of possible console select jumper configurations is shown in Table 2-11.

Table 2-11 Summary of Console Selection Jumper Configurations

Label	Console Selected	Console Not Selected
C1	Install jumper from wirewrap pins X to 1.	Install jumper from wirewrap pins X to 0.
C2	Install jumper from wirewrap pins X to 1.	Install jumper from wirewrap pins X to 0.

2.2.3 Configuring Channel Word Formats

2.2.3.1 General - Each DLV11-J SLU channel can be individually configured for number of data bits (7 or 8); even, odd, or no parity; 1 or 2 STOP bits, and baud rate (described in Paragraph 2.2.4). The serial character format is shown in Figure 2-6; jumper locations are shown in Figure 2-7; and a summary of possible character format jumper configurations is shown in Table 2-12.

2.2.3.2 Number of Data Bits – The serial character format for each channel can be configured for either seven or eight data bits. Three D (data) wirewrap posts are provided for the purpose of selecting the number of data bits per character for each channel. If seven data bits per character are desired, connect a jumper from wirewrap D pin X to pin 0. To configure eight data bits, connect the jumper from wirewrap D pin X to pin 1.

2.2.3.3 Number of STOP Bits – The serial character format for each channel can be configured for either one or two STOP bits. Configure one STOP bit operation by connecting a jumper between S (stop) wirewrap pin X and pin 0. To configure two STOP bits connect a jumper from wirewrap S pin X to pin 1.

NOTE

Two STOP bits are generally only required for use with Teletype® terminals.

2.2.3.4 Parity Inhibit - Even, odd, or no parity bit generation and detection can be configured for each channel. If no parity bit generation or detection is desired, delete the bit by connecting a jumper between P (parity) wirewrap pins X and 1. If a parity bit is desired connect P pins X and 0. Select even parity by connecting a jumper between E (even parity) wirewrap pin X and pin 1. Select odd parity by connecting a jumper between E pin X and pin 0.

NOTE

To prevent hardware damage within the channel, the E jumper must ALWAYS be installed. This is true regardless of the configuration of the P (parity) jumper.

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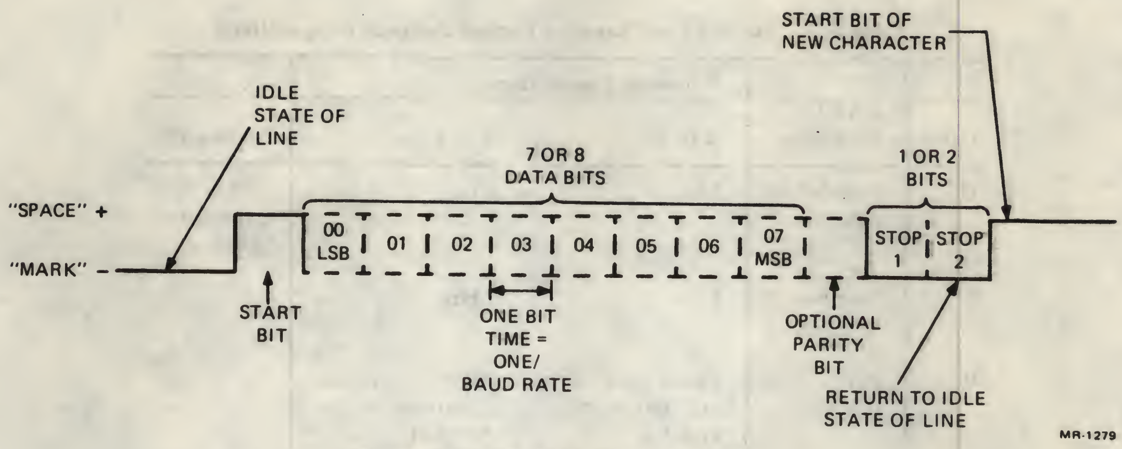


Figure 2-6 Serial Character Format for Transmitted and Received Data

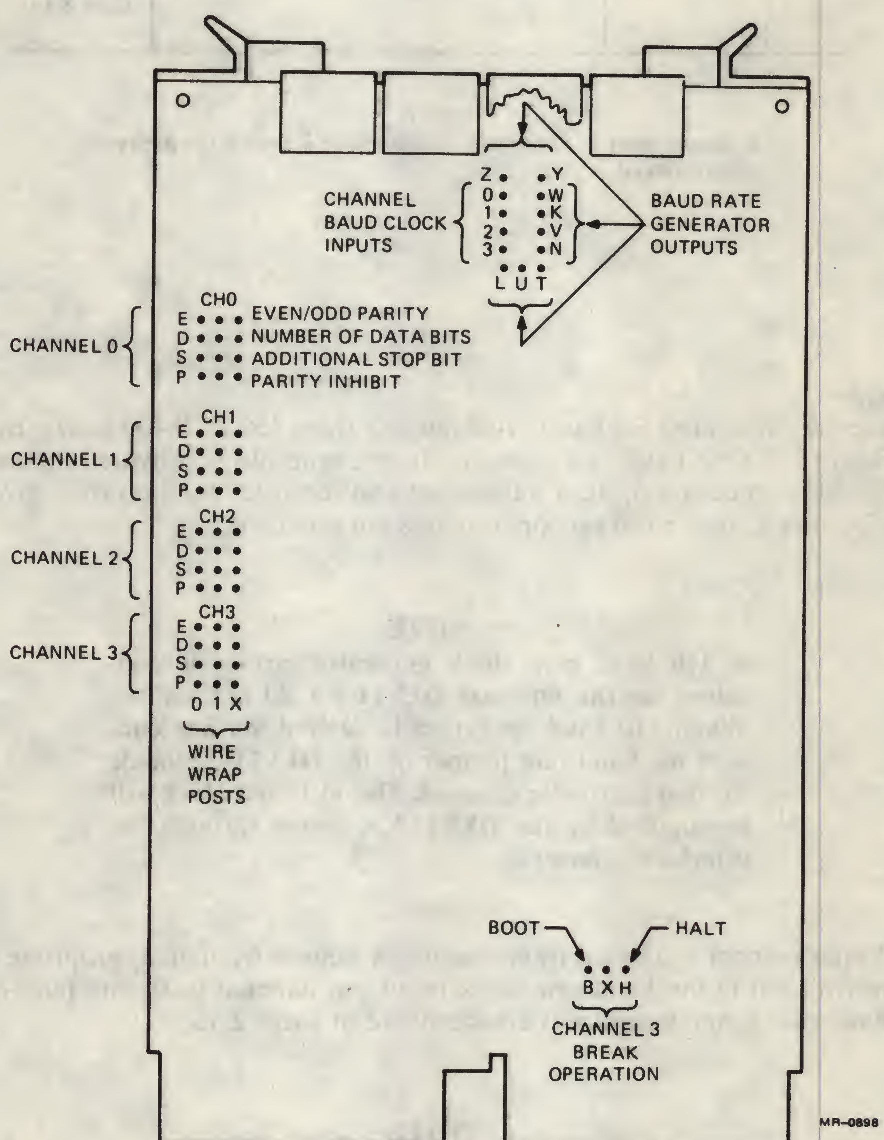


Figure 2-7 Character Format, Baud Rate and BREAK Response Jumper Locations

Table 2-12 Summary of Character Format Jumper Configurations

Label	UART Parameter	Wirewrap Connection X to 0	Wirewrap Connection X to 1	Comments
D	Number of data bits	7 bits	8 bits	LSB is transmitted first
S	Number of stop bits	1 bit	2 bits	
P	Parity inhibit	Parity generation and detection enabled	Parity generation and detection disabled	
E	Even parity enabled	Odd parity enabled	Even parity enabled	Requires P jumper connected from X to 0

NOTE
E jumper must be connected to either 0 or 1, even if the parity bit is disabled.

2.2.4 Baud Rate

Each channel can be configured for baud rates ranging from 150 to 38400 bits/s. Baud rate jumpers are shown in Figure 2-7. One baud rate clock input wirewrap pin is provided for each channel (pins 0–3 and channels 0–3 respectively). Both transmitter and receiver functions for a given channel operate at the same baud rate; split baud rate operation is not provided.

NOTE
A 110 baud rate clock generator circuit is contained on the optional DLV11-KA 20 mA option. When 110 baud operation is desired, do not connect the baud rate jumper on the DLV11-J module for that particular channel. The 110 baud clock will be supplied by the DLV11-KA option through the interface connector.

Configure baud rates (except 110 baud) by connecting a jumper from an appropriate baud rate generator output wirewrap pin to the baud rate clock input pin (labeled 0–3); one jumper is required for each channel. Baud rate generator outputs are identified in Table 2-13.

NOTE
If more than one channel requires the same baud rate, wirewrap jumpers may be daisy-chained.

Table 2-13 Baud Rate Generator Outputs

Wirewrap Pin Label	Baud Rate (bits/s)
U	150
T	300
V	600
W	1200
Y	2400
L	4800
N	9600
K	19200
Z	38400

2.2.5 Channel 3 BREAK Response

Channel 3 (normally used as the console device) can respond to a BREAK condition on the receive line such as when an operator presses the BREAK key on the associated terminal. The BREAK key transmits a continuous space signal which is detected by the DLV11-J circuits as a framing error. If no operation is desired, do not connect jumpers to the B, X, and H wirewrap pins. Boot and Halt response are described as follows.

Boot – This function causes the processor to restart operation by executing a bootstrap program. The bootstrap program starts at memory location 173000 whenever a BREAK condition occurs on the receive data line; this will occur only if processor power-up mode 2 is configured on the processor module. Otherwise, the processor will respond to its configured power-up mode.

Configure the bootstrap response by connecting a jumper from wirewrap pin X to B.

Halt – This function causes the processor to halt whenever a BREAK condition occurs on the receive data line. This operation will occur regardless of the processor power-up mode configured on the processor module. Whenever the processor halts, console octal debugging technique (ODT) microcode is invoked.

Configure the BREAK response by connecting a jumper from wirewrap pins X to H.

The location of the BREAK response jumpers is shown in Figure 2-7 and a summary of possible configurations is shown in Table 2-14.

Table 2-14 Channel 3 BREAK Operation Jumper Summary

BREAK Response Operation	Jumper Connection
Boot	Install jumper between wirewrap pins X and B.
Halt	Install jumper between wirewrap pins X and H.
No response	No jumper installed

2.2.6 Serial Line Signal Level Compatibility

2.2.6.1 General - Each SLU channel can be independently configured for signal line compatibility with EIA RS-422, RS-423, RS-232C, or 20 mA current loop devices. Configure each channel as directed in the following paragraphs. Jumper and pad locations are shown in Figure 2-8. Table 2-15 gives a summary of serial channel signal level compatibility configurations available on the module.

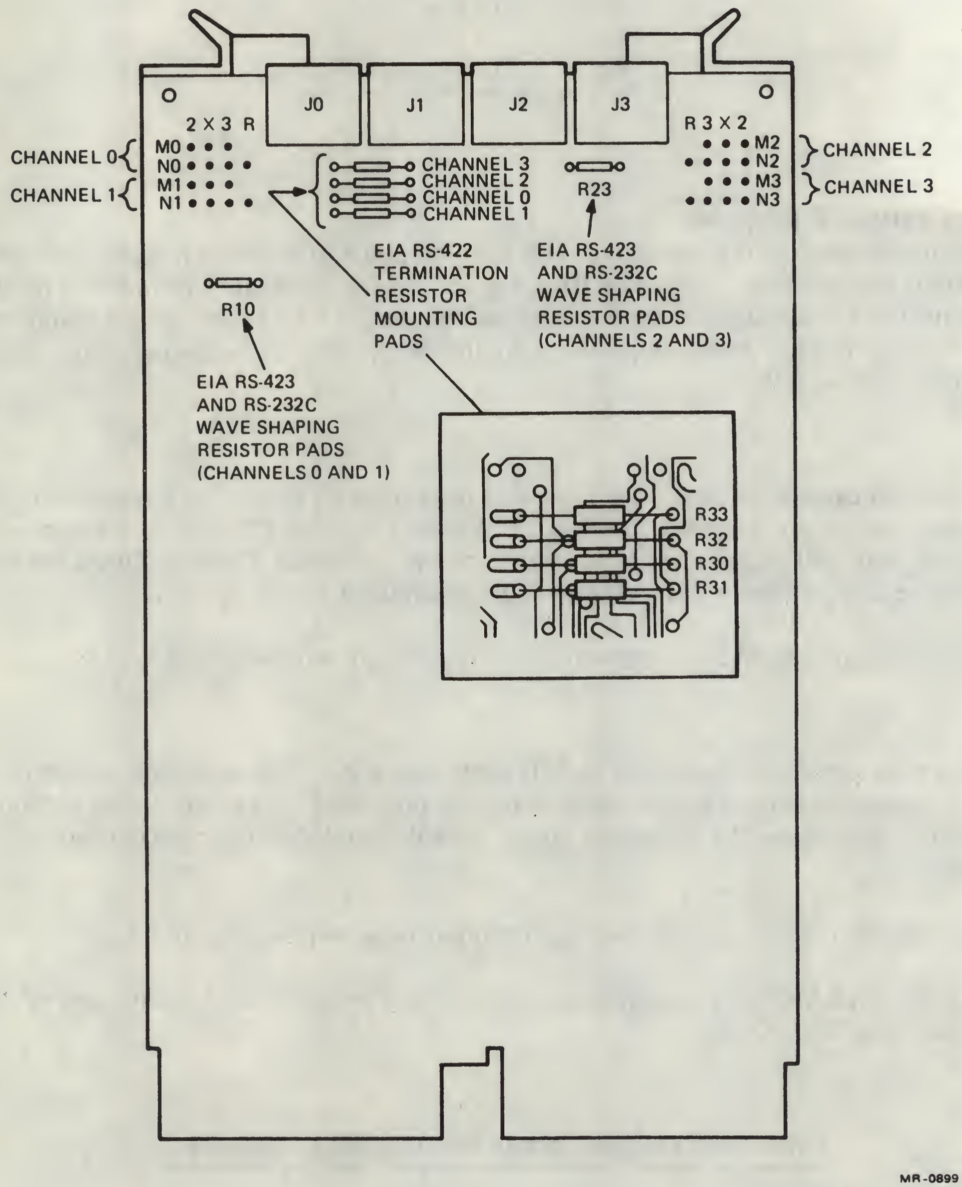


Figure 2-8 Serial Channel Signal Level Jumpers and Pads

Table 2-15 Summary of Serial Channel Signal Level Compatibility Configurations

Serial Channel Signal Level Modifiers	Serial Channel Signal Level: EIA RS-422	EIA RS-232C and RS-423	20 mA Current Loop (Required DLV11-KA Option)
M0–3 Jumpers	Connect wire-wrap pins X and 2.	Connect wire-wrap pins X and 3.	Connect wirewrap pins X and 3.
N0–3 Jumpers	Connect wire-wrap pins X and 2.	Connect wire-wrap pins X and 3.	Connect wirewrap pins X and R for program-controlled paper tape reader functionality.
Termination resistor (one per channel)	Install a 100 ohm, ¼ W, non-wire-wound, fusible resistor.	No resistor installed.	No resistor installed.
Wave shaping resistor, one per channel pair (channel pairs 0 and 1; 2 and 3).	Not required.	Install resistor from Table 2-16, ¼ W non-wirewound.	Install 22 kΩ non-wirewound resistor.

2.2.6.2 EIA RS-422 – To configure an SLU channel for EIA RS-422 signal levels, connect the M(M0–M3) and N(N0–N3) jumper wirewrap pin X of the desired channel to the respective wirewrap pin 2. Install (solder) a 100 ohm, ¼ W fusible resistor (non-wirewound) into the termination resistor mounting pads for the channel being configured. The resistor must be removed for any configuration other than EIA RS-422.

2.2.6.3 EIA RS-423 and RS-232C – To configure an SLU channel to be compatible with both the EIA RS-423 and RS-232C (which on the DLV11-J are met simultaneously), connect each M(M0–M3) and N(N0–N3) jumper X wirewrap pin of the desired channel to the respective wirewrap pin 3.

2.2.6.4 Slew Rates – The signal rise and fall time may be controlled on EIA RS-423 and RS-232C SLU channel configurations by installing (soldering) an appropriate value of non-wirewound, ¼ W resistor into the wave-shaping resistor pads provided (R10 and/or R23). An appropriate resistor value can be selected by referring to Table 2-16. The value of resistor R10 determines the slew rate of both channels 0 and 1 which are simultaneously set to the same value. Similarly, R23 controls the slew rate of both channels 2 and 3.

Table 2-16 EIA RS-423 and RS-232C Wave-Shaping Resistor Values

Baud Rate	Wave-Shaping Resistor
38.4K	22 kΩ
19.2K	51 kΩ
9.6K	120 kΩ
4.8K	200 kΩ
2.4K	430 kΩ
1.2K	820 kΩ
600	1 MΩ
300	1 MΩ
150	1 MΩ
110	See Note

NOTE

Determined by other channel of the 2-channel pair.

2.2.6.5 20 mA Current Loop – To configure an SLU channel for 20 mA current loop operation, connect the M(M0–M3) jumper pin X to pin 3 for the desired channel. If the 20 mA terminal contains a paper tape reader that can be program-controlled (such as a DEC-modified LT-33 Teletype or Teletype ASR-33 with LT33-MD modification kit), connect wirewrap jumper N(N0–N3) pin X to the respective pin R.

When the DLV11-KA 20 mA current loop option is connected to the channel interface connector, operating power for the option circuits is supplied by the DLV11-J. To configure a channel for 110 baud operation, enable the 110 baud rate clock on the DLV11-KA option and remove the baud rate selector jumper for the channel on the DLV11-J module. The clock needed by the DLV11-J is automatically supplied through the serial line connector cable.

2.3 INSTALLATION

2.3.1 Module Installation

CAUTION

DC power MUST be removed from the backplane during module insertion or removal.

2.3.1.1 Module Contact Finger (Pin) Identification – Digital plug-in modules all use the same contact finger (pin) identification system. The LSI-11 I/O bus is based on the use of double-height modules which plug into a 2-slot bus connector, each slot containing 36 lines (18 lines each on component and solder sides of the circuit board).

Slots, shown as Row A and Row B in Figure 2-9, include a numeric identifier for the side of the module. The component side is designated as side 1 and the solder side is designated as side 2. Letters ranging from A to V (excluding G, I, O, and Q) identify a particular pin on a side of a slot. Hence, a typical pin is designated as:

B E 2

Slot (Row) Identifier

Module Side Identifier – Solder Side

Pin Identifier Pin E

Note that the positioning notch between the two rows of pins mates with a protrusion on the connector block for correct module orientation.

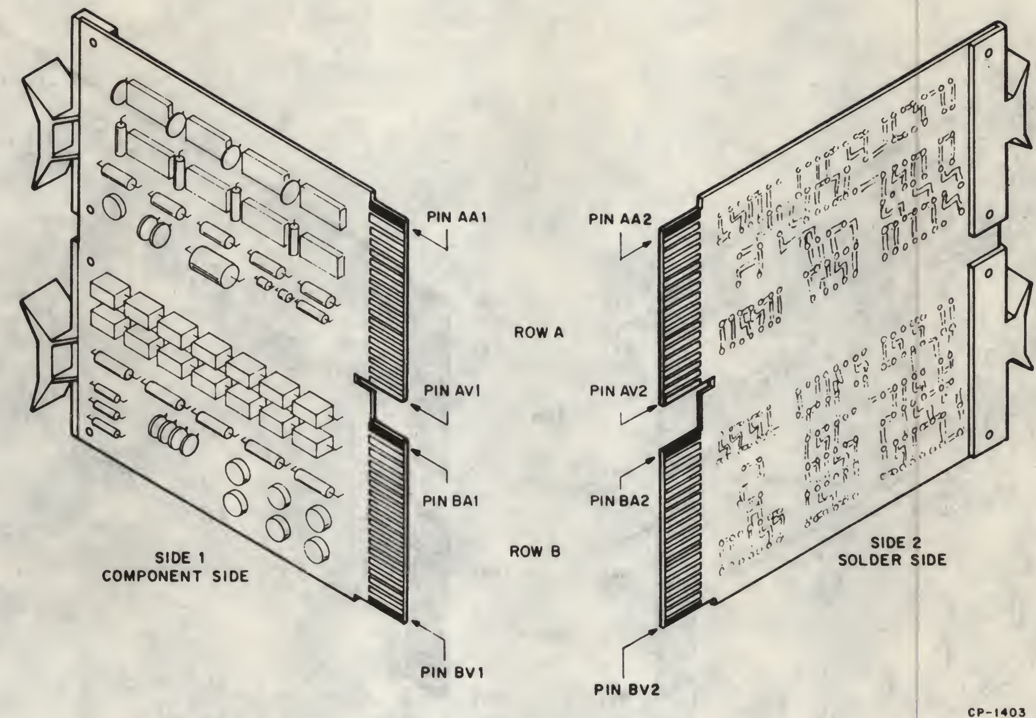


Figure 2-9 Module Contact Finger Identification

CAUTION

The module and/or backplane connector blocks can be damaged if the module is installed backwards. Ensure that the component side of the module faces in the same direction as other LSI-11 system modules.

Quad-height modules are similarly pin-numbered. They are identified in Figure 2-10.

Individual connector pins, viewed from the underside (wiring side) of a backplane, are identified as shown in Figure 2-11. Only the pins for one bus location (two slots) are shown in detail. This pattern of pins is repeated eight times on the H9270 backplane.

2.3.1.2 Module Priority - DLV11-J module interrupt priority is dependent on module electrical position in the LSI-11 backplane. Refer to the *Microcomputer Handbook,* Section 1, Chapter 3 for device priority considerations.

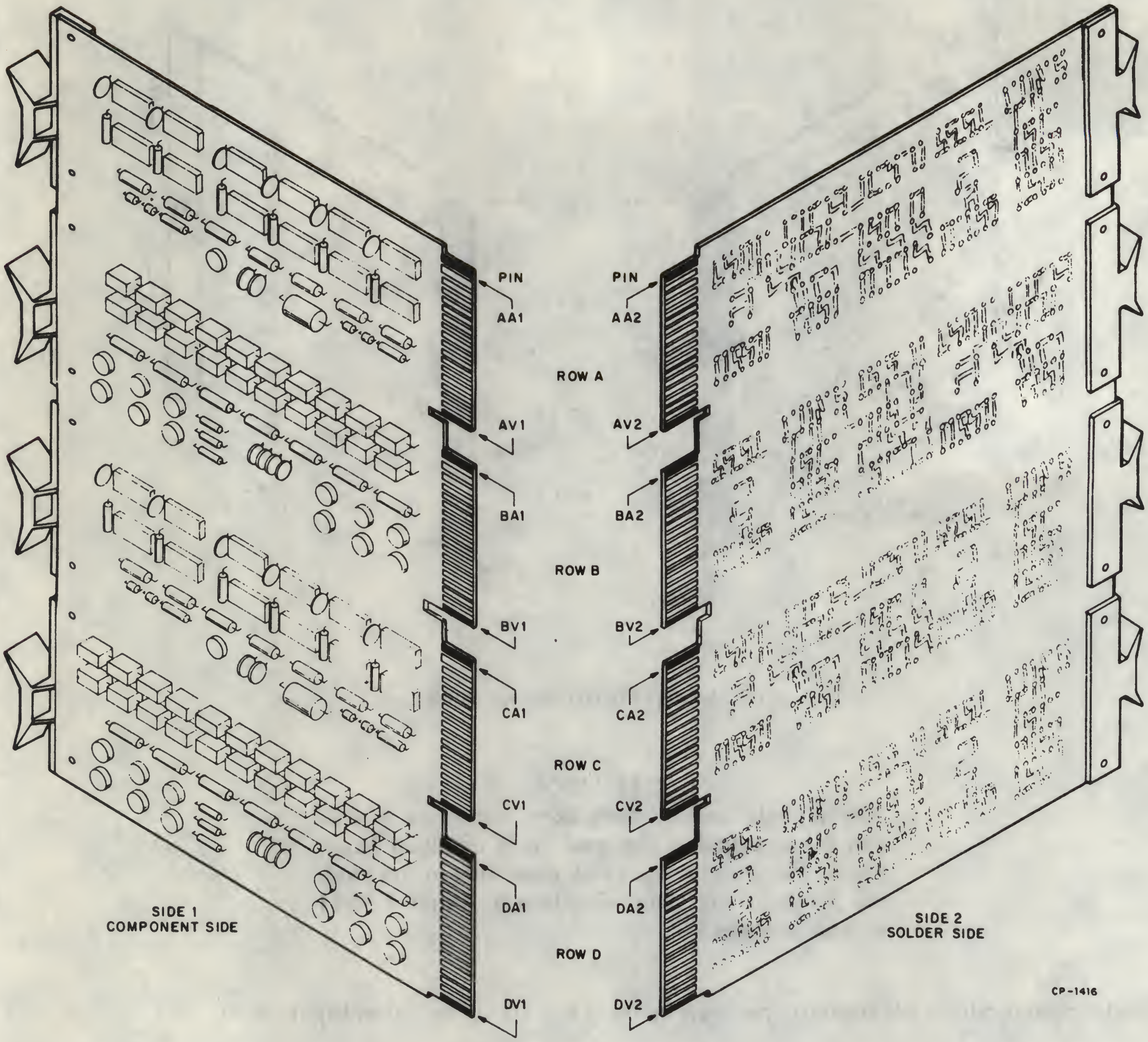


Figure 2-10 Quad Module Contact Finger Identification

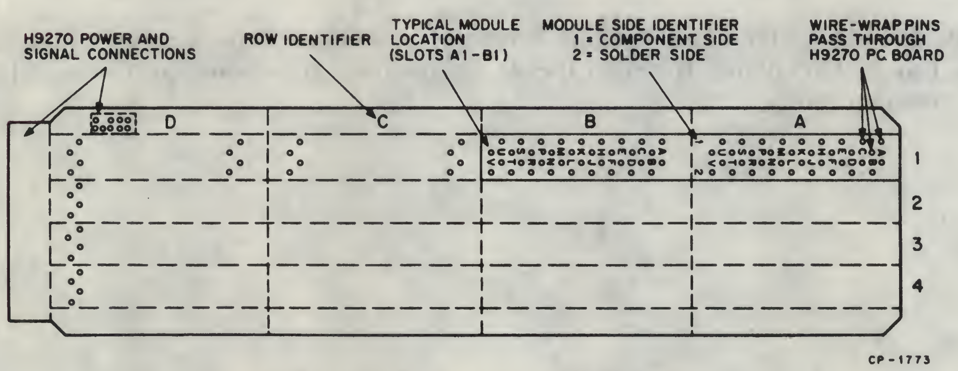


Figure 2-11 LSI-11, PDP-11/03 Backplane
Module Pin Identification

2.3.2 Cabling Considerations

When interconnecting equipment that meets compatible, but different EIA standards, the performance of the channel is limited by the least efficient EIA specification. Specifically EIA RS-232C/RS-423 mixed connections are limited to EIA RS-232C performance capabilities and EIA RS-423/RS-422 mixed connections are limited to EIA RS-423 performance capabilities. This consideration is critical when choosing baud rates and cabling lengths for the computer system. Figure 2-12 gives the relationship between baud rate and cable length for both EIA RS-423 and RS-422 specifications. Remember, when connecting equipment that adheres to EIA RS-232C specifications, the baud rate is limited to 20K bits per second with a maximum cable length of 50 feet.

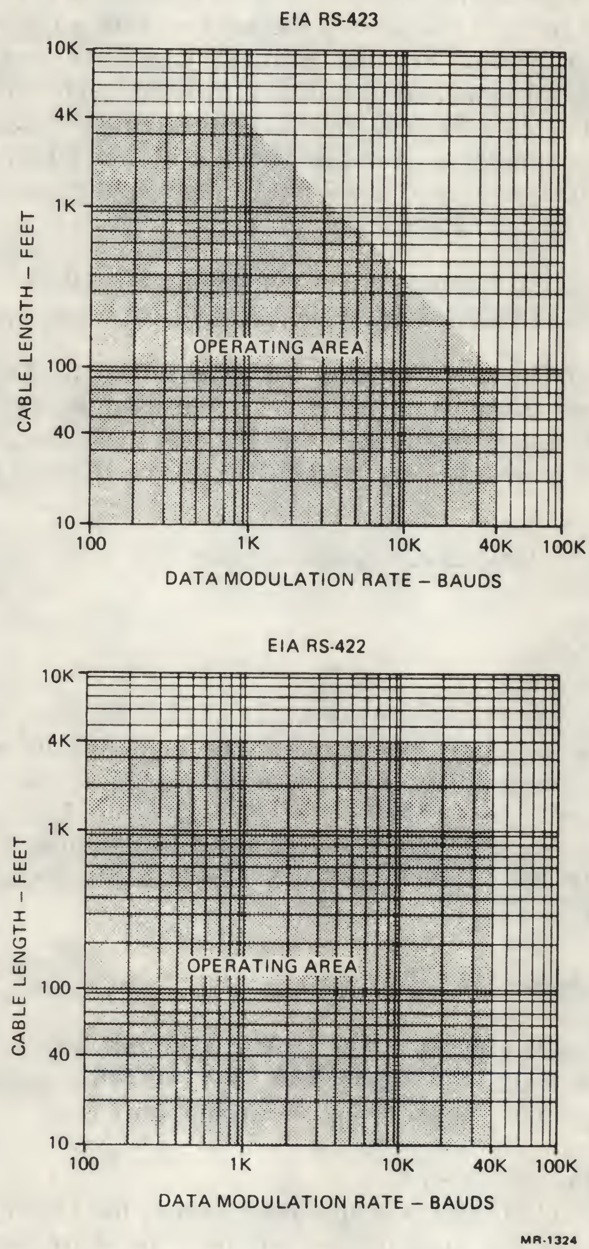


Figure 2-12 Baud Rate vs Cable Length

When configuring the slew rate for the channels (for EIA RS-423/RS-232C), the value of R10 (channels 0 and 1) and R23 (channels 2 and 3) may be changed to meet specifications shown in Table 2-16. Because the channels are configured in pairs, the highest baud rate of the channel pair limits the cable length of both channels. This fact must be taken into consideration when using high baud rates over long cable lengths. The DLV11-J is factory-configured with a 22K ohm slew rate resistor which allows operation at all baud rates, but limits cable length to 100 ft.

2.3.3 Cable Installation

Table 2-17 and Figure 2-13 give the part numbers, applications and lengths of the cabling and options available for the DLV11-J module.

2.3.3.1 Modem Operation Cabling - The DLV11-J module operates in the Data Leads Only mode; it does not monitor EIA control lines. It will supply the modem with a continuous true logic level on both the request-to-send (RTS) and data terminal ready (DTR) control lines, allowing the DLV11-J to operate with modems equipped with manual operation provisions (such as the Bell 103A data set with 804B auxiliary set). Figure 2-14 shows the BC21B-05 cable. The cable is used to connect the DLV11-J module to a modem or acoustic coupler as shown in Figure 2-15. The DLV11-J device connector is an AMP 87133-5 receptacle which is configured in a 2-pin by 5-pin configuration. The modem connector is a standard EIA RS-232C 25-pin connector.

2.3.3.2 Local Terminal Operation Cable - When connecting the DLV11-J to local terminals, two methods may be used as shown in Figure 2-16. When using 20 mA terminals see Figure 1-4.

2.3.3.3 DLV11-J to DLV11-J Operation Cabling - Digital offers the BC20M-50 cable (50 ft) for DLV11-J to DLV11-J operation as shown in Figure 2-17. Because longer cables usually require routing without connectors attached, it is encouraged that the user make cables for lengths greater than fifty feet. Cable material must adhere to EIA RS-422/423 specifications. Recommended cable material is as follows.

2 twisted-pair, individually shielded 22 to 24 gauge wire
mutual capacitance 20 pF/ft
stray capacitance 40 pF/ft
resistance < 30 ohms/1000 ft

The connectors on the DLV11-J module are AMP 87272-8 (2-pin by 5-pin on 0.1 inch centers). These connectors can mate with a wide variety of low cost cables including 10-conductor flat cable. Cable retention in the module connector is provided by use of locking clip contacts (AMP PN 87124-1; DEC P/N 12-14267-00). The cable receptacle (AMP PN 87133-5, DEC PN 12-14268-02) will not pull out of the module connector if the cable is pulled; however, it is easily removed if the receptacle is pulled back. Note that keying (AMP PN 87179-1, DEC PN 12-15418-00) is provided (pin 6 removed) to allow "active" cable indexing.

Cable wiring instructions can be seen in Figure 2-18.

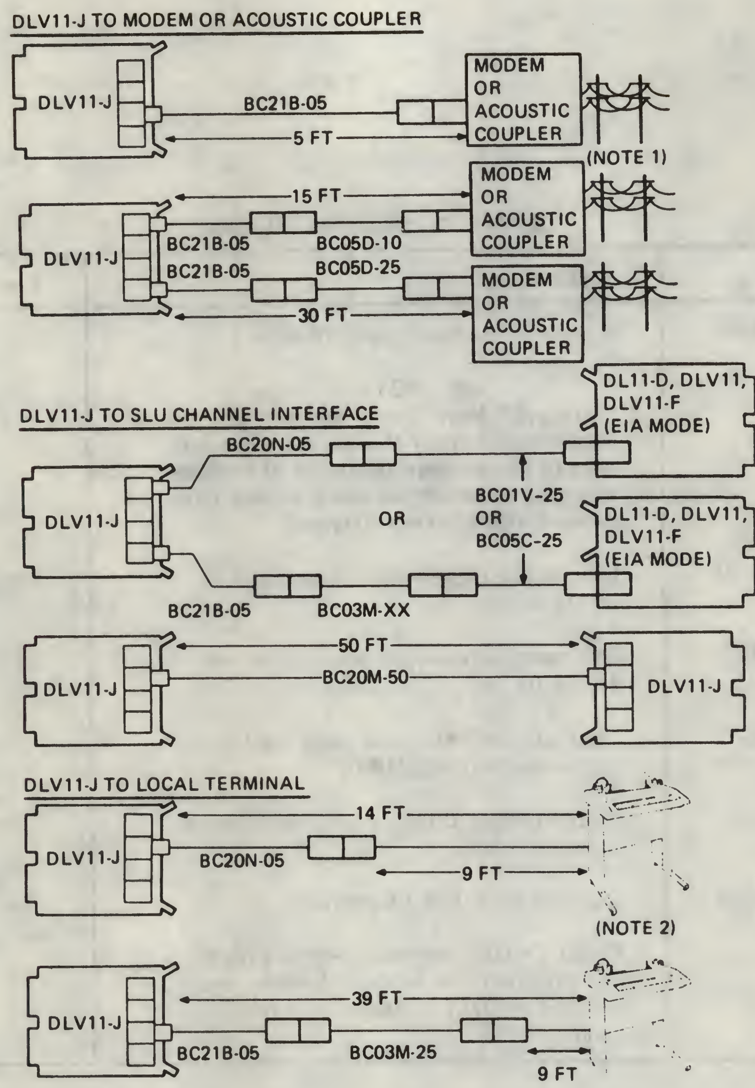
2.3.3.4 DLV11-J to SLU Module Cabling – The DLV11-J module may be linked to serial line units that are EIA-compatible (such as the DL11-D, DLV11, DLV11-F, etc., when configured for EIA operation). The two cabling configurations possible are shown in Figure 2-19.

2.4 CHECKOUT/ACCEPTANCE TESTS

A diagnostic program is available to verify proper operation of the DLV11-J module. The program will run on any LSI-11-based system containing a minimum of 4K of memory. For data loopback tests to be performed, the diagnostic requires the H3270-A option (four diagnostic loopback plugs) to be inserted into the module's four peripheral device connectors. To configure the DLV11-J module for testing, remove dc power and insert the H3270-A diagnostic loopback plugs. The computer may then be powered up, and the program loaded and started.

Table 2-17 Definition of Cables

Cable	Application	Length
BC21B-05	Modem or acoustic coupler operation NOTE **"Strapped" logic levels are provided on data terminal ready (DTR) and request to send (RTS) to allow operation of modems with manual provisions (such as Bell 103A data set with 804B auxiliary set).**	1.5 m (5 ft)
BC05D-10	Extension cable used in conjunction with BC21B-05	3 m (10 ft)
BC05D-25	Extension cable used in conjunction with BC21B-05	7.6 m (25 ft)
BC03M-25	"Null Modem" extension cable used in conjunction with BC21B-05	7.6 m (25 ft)
BC20N-05	"Null Modem" cable for local terminal connection	1.5 m (5 ft)
BC20M-50	DLV11-J to DLV11-J Operation	15 m (50 ft)
H3270-A	Four DLV11-J diagnostic loopback plugs – One plug required for each channel; four required per DLV11-J module to run diagnostic.	



NOTES:

1. MODEM USED IS A "MANUAL TYPE" SUCH AS BELL 103A WITH 804B.
2. DEC EIA RS-232C TERMINALS (VT52, LA36, LS120, ETC.) COME EQUIPPED WITH A 9 FT CABLE. NON-DEC EIA RS-232C TERMINALS ARE CONNECTED SIMILARLY EXCEPT 9 FT OF LENGTH MUST BE DEDUCTED FROM THE TOTAL CABLE LENGTH.

Figure 2-13 DLV11-J Cabling Summary

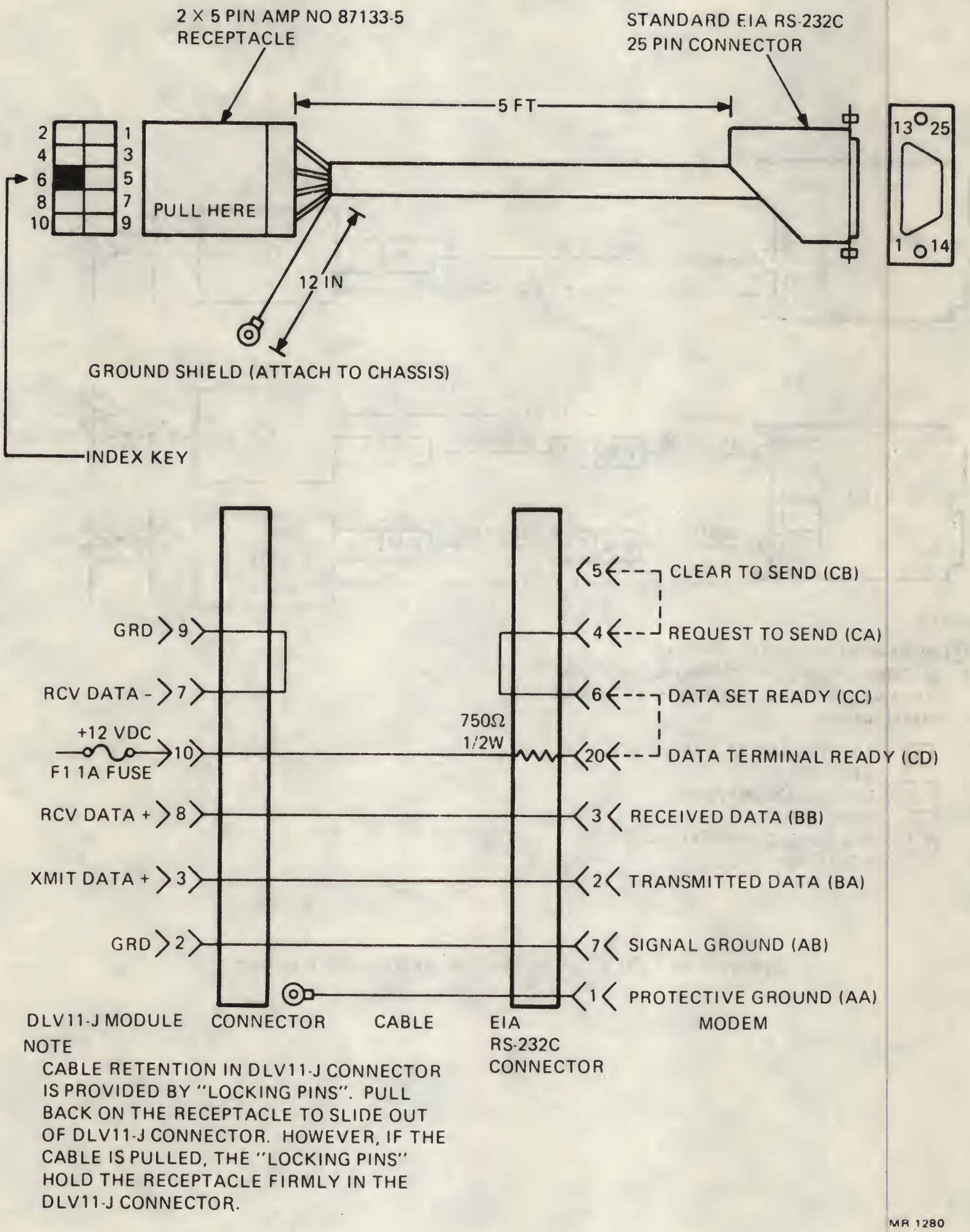
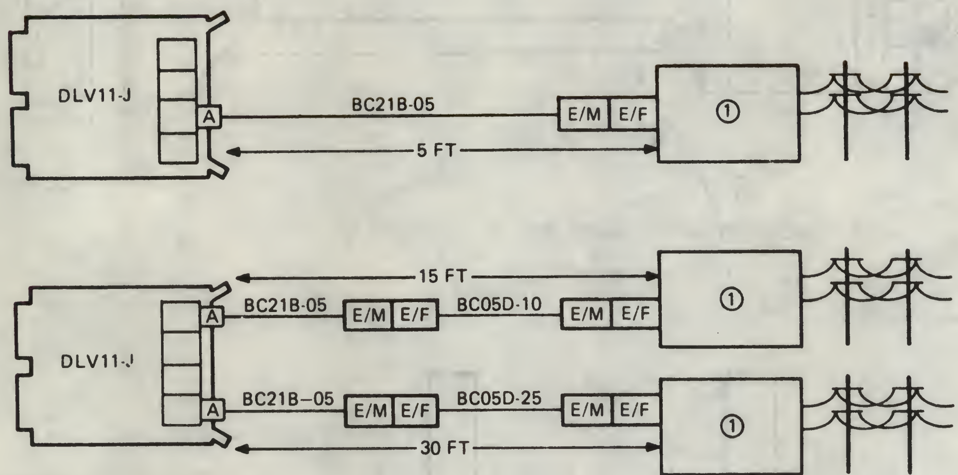


Figure 2-14 BC21B-05 Peripheral Device Cable



NOTES:

1 MODEM OR ACOUSTIC COUPLER.
MODEMS SHOWN ARE "MANUAL" MODEMS SUCH AS BELL 103A DATA SETS WITH 804B AUXILIARY SET.

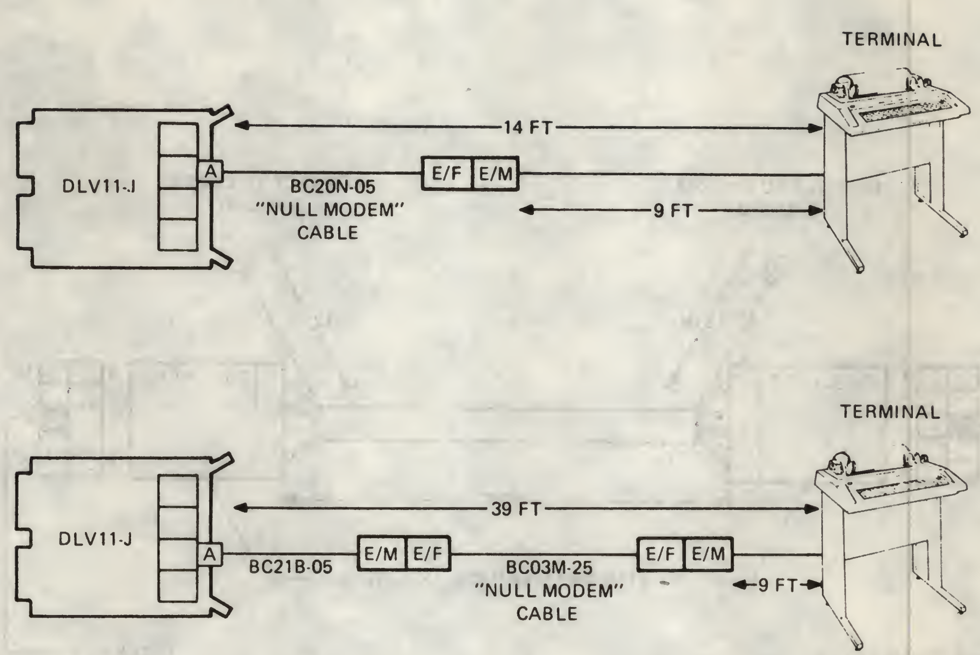
A = 2 X 5 PIN AMP NO 87133-5 CONNECTORS

E/M = EIA RS-232C 25 PIN MALE CONNECTORS

E/F = EIA RS-232C 25 PIN FEMALE CONNECTORS

MR-1281

Figure 2-15 DLV11-J to Modem or Acoustic Coupler



NOTES

TERMINALS SHOWN ARE DEC EIA RS-232C TERMINALS (SUCH AS VT52, LA36, LS120, ETC.)

DEC TERMINALS ARE CONSTRUCTED WITH 9 FOOT CABLES, WHEN USING NON-DEC EIA RS-232C TERMINALS DEDUCT 9 FEET FROM THE TOTAL CABLE LENGTH.

$\boxed{\text{A}}$ = 2 X 5 PIN AMP NO 87133-5 CONNECTORS

$\boxed{\text{E/M}}$ = EIA RS-232C 25 PIN MALE CONNECTORS

$\boxed{\text{E/F}}$ = EIA RS-232C 25 PIN FEMALE CONNECTORS

MR-1282

Figure 2-16 Local Terminal Cabling

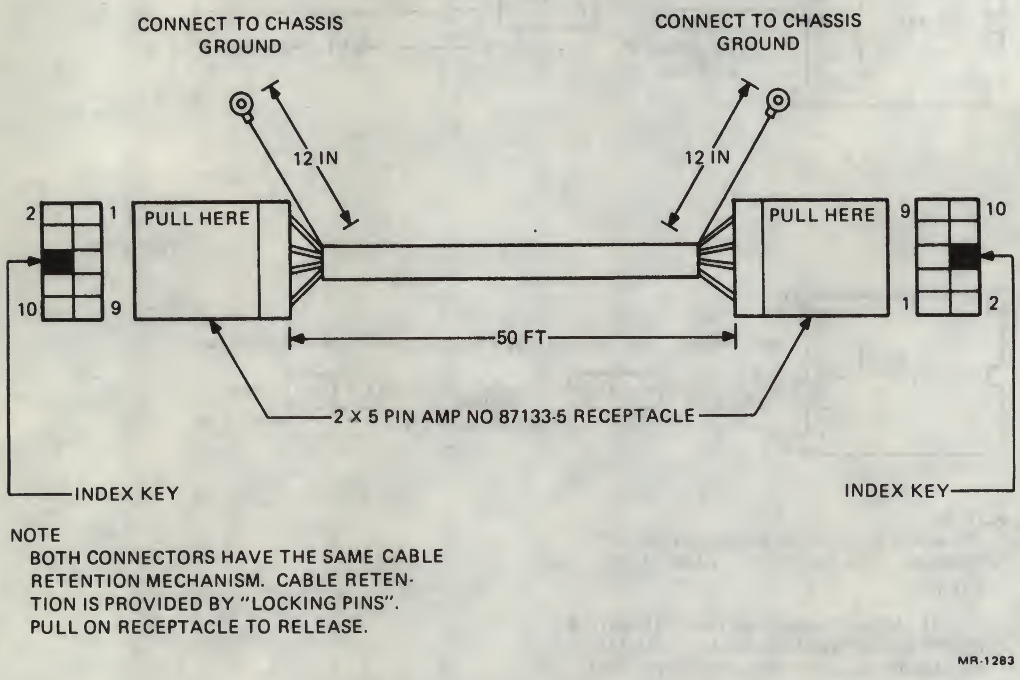


Figure 2-17 BC20M-50 DLV11-J to DLV11-J Cable

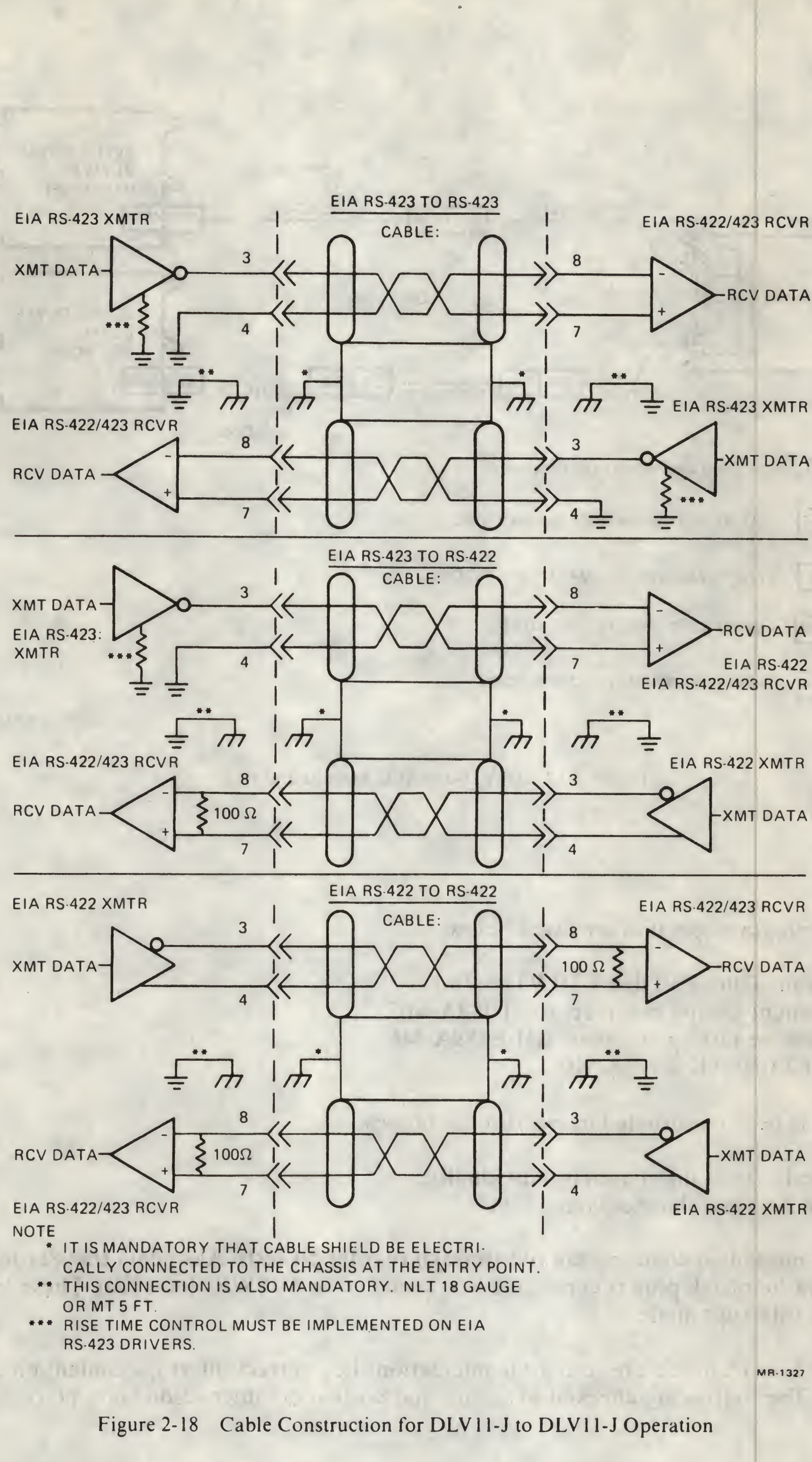


Figure 2-18 Cable Construction for DLV11-J to DLV11-J Operation

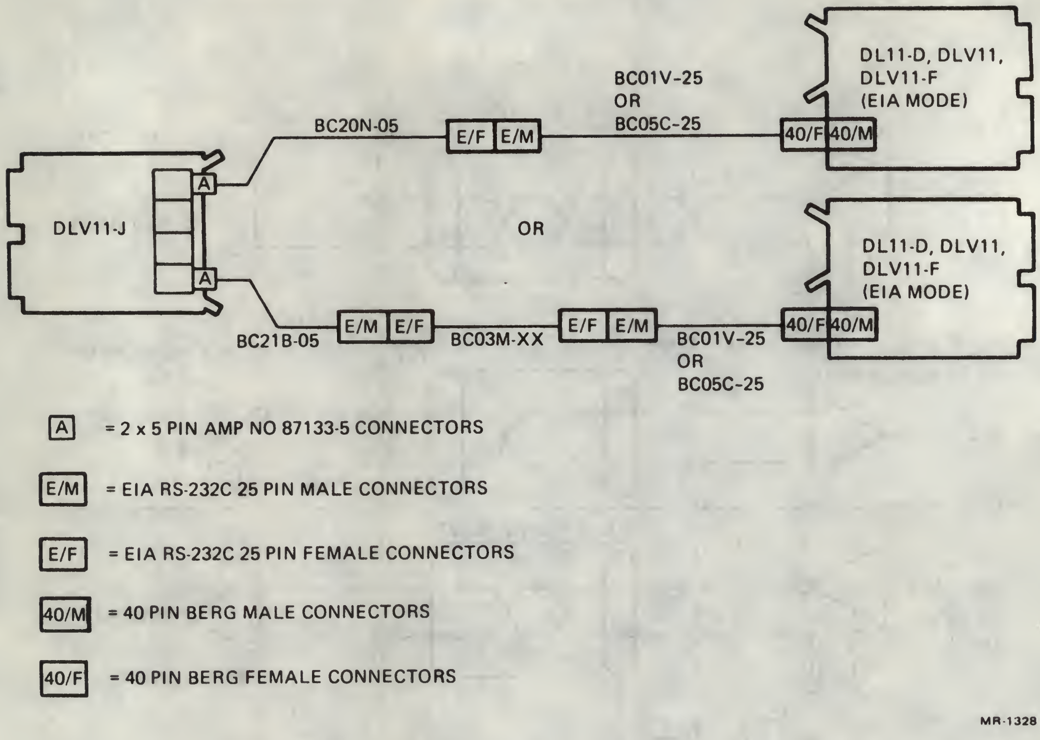


Figure 2-19 DLV11-J to SLU Module Cabling

The diagnostic program specifics are listed below.

Program Title: CVDLAA DLV11-J Test
Document Listing Number: AC-E188A-MC
Microfiche Listing Number: AH-E189A-MC
Paper Tape: AK-E190A-MC

The program has been constructed in two distinct phases:

Phase 1 – Tests the channels individually
Phase 2 – Tests channel interaction.

In phase 1, the individual channels are run through register bit tests. Also, data transfer tests are executed if the data loopback plug is connected and specified in $USWR (loc 1220). These tests are run in the Flag and Interrupt modes.

In phase 2, the four channels are tested for interaction; i.e., correct interrupt contention and correct buffer loading. The buffers are checked to ensure that no channel interaction takes place when data is transferred.

CHAPTER 3
PROGRAMMING

3.1 GENERAL

All programmed operations involving the DLV11-J are via 16 device registers contained on the module. Four device registers are provided for each of the four channels. Each device register is assigned a unique device address, as described in Chapter 2. Device register formats for each channel are identical; therefore, similar routines can be used for all four channels.

This chapter describes register addressing, register formats, interrupts, and console device operational requirements.

3.2 DEVICE REGISTER ADDRESSING

DLV11-J device registers generally occupy 16 contiguous word locations; however, the module can be configured with channel 3 as the console device. When this is done, channel 3 device register addresses will always be assigned four contiguous word addresses starting at 177560; channels 0 through 2 device register addresses will then occupy 12 contiguous word addresses starting at a base address (the factory or user-configured address for channel 0 RCSR device register).

NOTE

Channel 3 can be used as the console device only when certain base addresses are used. These addresses are 176500 (factory-configured), 176540 or 177500.

Within any one of four DLV11-J channels, the least significant octal digit of the address designates a specific register, as follows.

Octal Address	Device Register	Function
MSD LSD		
XXXXX0	RCSR	Receiver control/status register
XXXXX2	RBUF	Receiver data buffer
XXXXX4	XCSR	Transmitter control/status register
XXXXX6	XBUF	Transmitter data buffer

Channel addresses are sequential in increments of 10_8. The user can configure a module to a specific base address in increments of 40_8; this procedure is described in Chapter 2. The base address is the channel 0 RCSR address. All addresses follow sequentially starting at the base address. When channel 3 is configured for console device operation, the following device addresses are assigned for LSI-11 system compatibility.

Console Device Register Address	**DLV11-J Register**
177560	Channel 3 RCSR
177562	Channel 3 RBUF
177564	Channel 3 XCSR
177566	Channel 3 XBUF

3.3 INTERRUPT VECTORS

Eight interrupt vectors are assigned to each DLV11-J module. Two interrupt vectors (receiver and transmitter) per channel are used for each of the four channels. The vectors are in sequence, starting at a base vector assigned as the channel 0 receiver interrupt vector and progressing upward in increments of 4_8. However, when channel 3 is configured for use as the console device, the following vectors are enabled.

Console Device Interrupt Vector	**DLV11-J Interrupt Vector**
60	Channel 3 Receiver
64	Channel 3 Transmitter

3.4 WORD FORMATS

Four word formats, one for each device register, are applicable for each DLV11-J channel. Word formats are shown in Figure 3-1 and are described in Table 3-1.

3.5 INTERRUPTS

Each DLV11-J channel can generate both receiver and transmitter interrupts. Interrupt priority of the DLV11-J is established by the module's electrical position along the LSI-11 bus with respect to other devices that are capable of requesting interrupts. The module electrically closest to the processor receives highest interrupt priority; the module farthest from the processor receives lowest interrupt priority.

Interrupt priority within the DLV11-J module is also structured. Interrupt priority is as follows.

Interrupt Priority	**Requesting Function**
1 (highest)	Channel 0 Receiver
2	Channel 1 Receiver
3	Channel 2 Receiver
4	Channel 3 Receiver
5	Channel 0 Transmitter
6	Channel 1 Transmitter
7	Channel 2 Transmitter
8 (lowest)	Channel 3 Transmitter

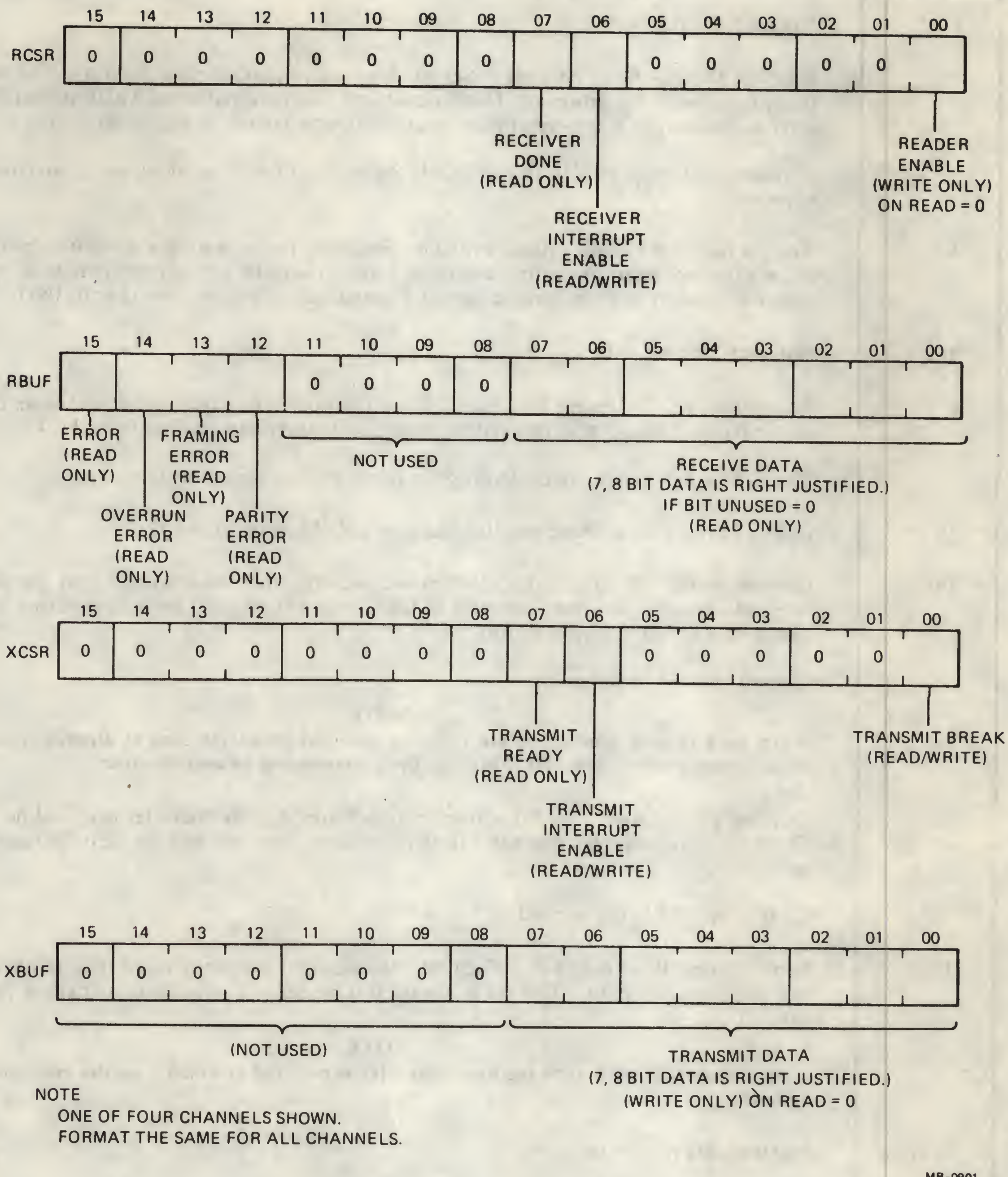


Figure 3-1 DLV11-J Device Register Word Format

Table 3-1 DLV11-J Word Formats

Word	Bit(s)	Function
RCSR	8–15	Not used. On read = 0.
	7	Receiver Done – Read only bit – Set when an entire character has been received and is ready for input to the processor. This bit is automatically cleared when RBUF is read, when INIT is asserted (on power-up or reset instruction), or when reader enable bit is set. If receiver interrupt enable (bit 6) is set, the setting of receiver done starts an interrupt sequence.
	6	Receive Interrupt Enable - Read/write bit - Set under program control when it is desired to allow a receiver interrupt sequence to occur when a character is ready for input to the processor (signified by receiver done being set). Cleared under program control or by INIT.
	1–5	Not used. On read = 0.
	0	Reader Enable - Write only bit - Setting this bit advances the paper tape reader on an LT-33 terminal one character at a time and the setting of this bit clears receiver done (bit 7). The DLV11-KA 20 mA current loop option is required for operation of this bit.
RBUF	15	Channel Error Status - Read only bit - Logical OR of bits 14, 13 and 12.
	14	Overrun Error - Read only bit - When set, indicates that the reading of the previously received character was not completed (RCVR done not cleared) prior to receiving a new character. The first character is "lost." Cleared by INIT being asserted. NOTE **When back-to-back characters are received, one full character time is allowed from the instant when receiver done (bit 7) is set to the occurrence of an overrun error.**
	13	Framing Error - Read only bit - When set, indicates that the character read had no valid STOP bit. This indicates that the currently received character and the next character are invalid. Cleared by INIT being asserted.
	12	Parity Error - Read only bit - When set, indicates that the parity received does not agree with the expected parity. This bit is always 0 if no-parity operation is configured for the channel. NOTE **Error bits remain valid until the next character is received at which time the error bits are updated.**
	8–11	Not used. On read = 0.
	0–7	Data bits - Read only - Contains seven or eight data bits in a right-justified format. Bit 7 = 0 when seven data bits are enabled.
XCSR	8–15	Not used. On read = 0.
	7	Transmit Ready - Read only bit - Set when XBUF is empty and can accept another character for transmission. It is also set by INIT during the power-up sequence or during a reset instruction. If transmitter interrupt enable (bit 6) is set, the setting of transmit ready will start an interrupt sequence.

Table 3-1 DLV11-J Word Formats (cont)

Word	Bit(s)	Function
	6	Transmit Interrupt Enable – Read/write bit – Set under program control when it is desired to generate a transmitter interrupt request (when transmitter is ready to accept a character for transmission). The bit is cleared under program control, during power-up sequence, or reset instruction.
	1–5	Not used. On read = 0.
	0	Transmit Break – Read/write bit – Set or reset under program control. When set, a continuous space level is transmitted. However, transmit done and transmit interrupt enable can still operate allowing software timing of the Break signal. When not set, normal character transmission can occur. Cleared by INIT being asserted.
XBUF	8–15	Not used. On read = 0.
	0–7	Data bits – Write only – Contains seven or eight right-justified data bits. Loaded under program control for serial transmission. On read = 0.

An interrupt can be generated by a device function only when its interrupt enable bit is set (described in Table 3-1 for RCSR and XCSR bit 6). If the interrupt enable bit is set, an interrupt request will be issued by a DLV11-J channel when its DONE (receiver) or READY (transmitter) bit becomes set (described in Table 3-1 for RCSR and XCSR bit 7). Setting the DONE or READY bit indicates that the function (for a specific SLU channel transmitter or receiver) is ready for service – a data transfer. When the processor acknowledges the DLV11-J's interrupt request (according to bus protocol), the DLV11-J places the appropriate interrupt vector onto the bus. The processor then inputs the vector and obtains the appropriate service routine PC (program counter, or starting address) and PS (processor status word) from the memory locations addressed by the vector and vector plus 2, respectively. Thus, two memory locations are referenced by the interrupt vector for gaining access to the service routine of the interrupting device.

3.6 CONSOLE DEVICE

For a device to function as the console device it must be able to transmit and receive ASCII characters and to use the standard console device register and interrupt vectors as follows.

Address	Dedicated Console Device Function
000060	Receiver interrupt vector
000064	Transmitter interrupt vector
177560	RCSR
177562	RBUF
177564	XCSR
177566	XBUF

When the boot response is selected, the BREAK key causes the system to respond as though a power-up sequence were being executed. This feature is most useful when the processor module is configured for power-up mode 2. This power-up mode causes the processor to start program execution at memory location 173000 (typically PROM-resident). Thus, pressing the BREAK key will cause the processor to execute a resident program starting at 173000.

When the halt response is selected, the BREAK key causes the processor to print the halt (PC + 2) address and the "@" octal debugging technique (ODT) prompt character on the console terminal, and halt. The operator can then communicate with the processor using console ODT commands.

If the console device terminal is equipped with a BREAK key, it can be used to boot the system, cause the processor to halt (console emulator mode) or have no response; one of these BREAK functions can be selected when configuring the DLV11-J module prior to installation in the system backplane, as directed in Chapter 2. Pressing the BREAK key generates a continuous space condition which is detected by the DLV11-J as a framing error. Note that only channel 3 can respond to the BREAK key by booting or halting the system.

CHAPTER 4
TECHNICAL DESCRIPTION

4.1 GENERAL

The DLV11-J is designed to interface equipment that transmits and receives data over EIA-compatible data lines or 20 mA current loop data lines to an LSI-11 bus. When configured for EIA signal level compatibility, the DLV11-J transmits and receives EIA signal levels over the peripheral device interface cable. When configured for 20 mA current loop operation, the DLV11-J can support current loop devices including those which contain paper tape readers which are program controlled (such as DEC LT-33 terminals or Teletype ASR33 with LT33-MD modification kit installed). A general block diagram of the DLV11-J module is shown in Figure 4-1.

NOTE
Detailed schematics may be obtained by ordering field maintenance print set no. MP00586.

4.2 MODULE FUNCTIONS

The DLV11-J 4-channel asynchronous serial line interface module takes data from the LSI-11 bus and converts it to the timing, character format, and signal level required by the user's peripheral device. Conversely, it assembles inputs from the peripheral device and converts them to the format required by the processor. The computer program can address any of the four device registers within each channel to transfer data and status information. It also can enable the interface module to generate interrupts. When a peripheral device requires service, the interface module will, if enabled, interrupt the program and provide a vector to the necessary service routine.

4.2.1 Operational Overview

Data passes through three main circuits when moving to and from a peripheral device (see Figure 4-2). During computer output operations, parallel data is taken off the LSI-11 bus by the bus interface circuit and placed on the module's internal tri-state bus. The data on the tri-state bus enters a data buffer, where it is serialized and formatted for the peripheral device. The data enters the peripheral interface which changes the data from TTL (transistor-to-transistor logic) to EIA-compatible bipolar levels. The data leaves the module on an interface cable and enters the user's peripheral device. When using 20 mA current loop signals an external option (DLV11-KA) is placed between the DLV11-J peripheral interface output and the 20 mA device. Data coming into the computer from the peripheral device goes through the main circuits of the module in the reverse order.

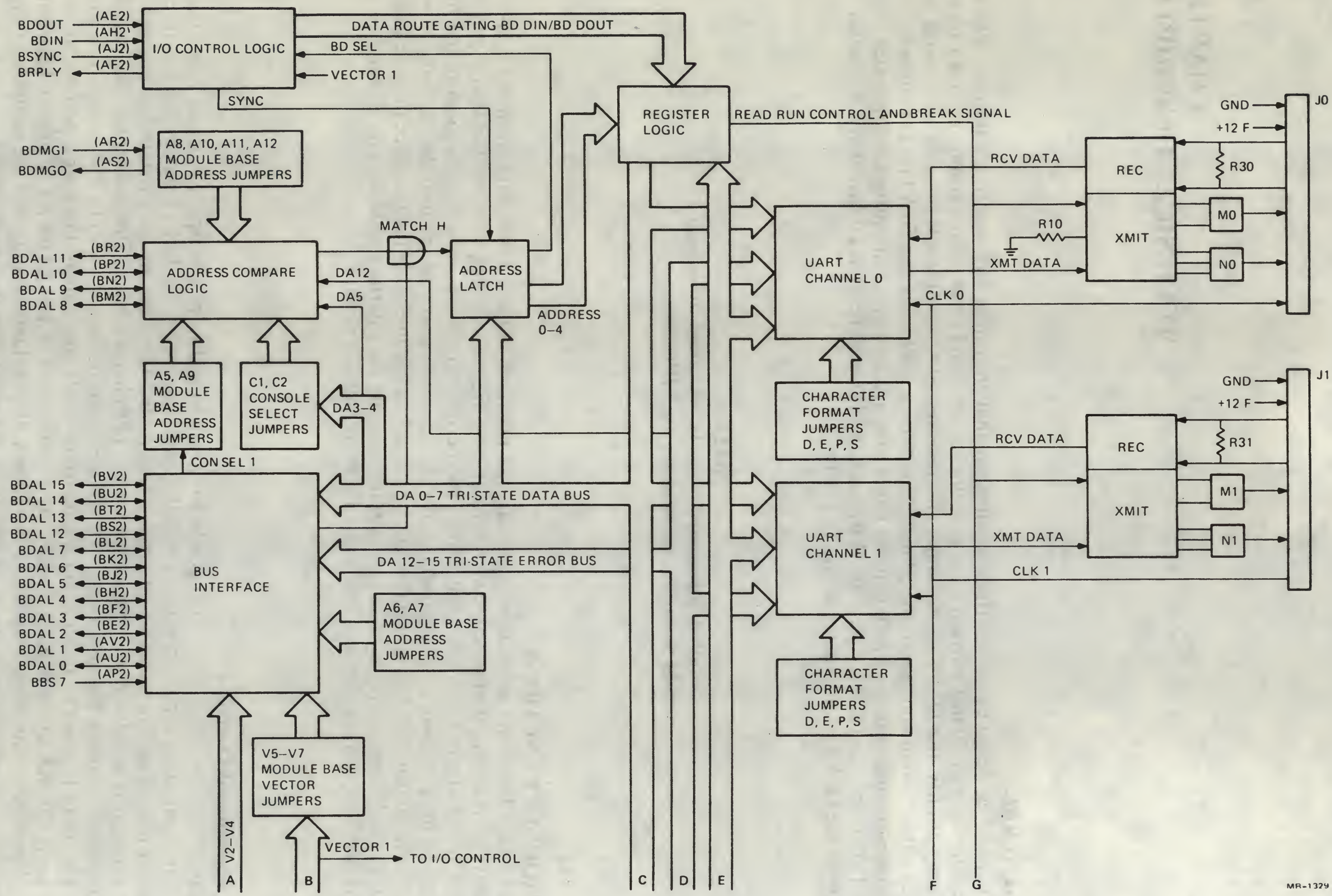


Figure 4-1 DLV11-J Block Diagram (Sheet 1 of 2)

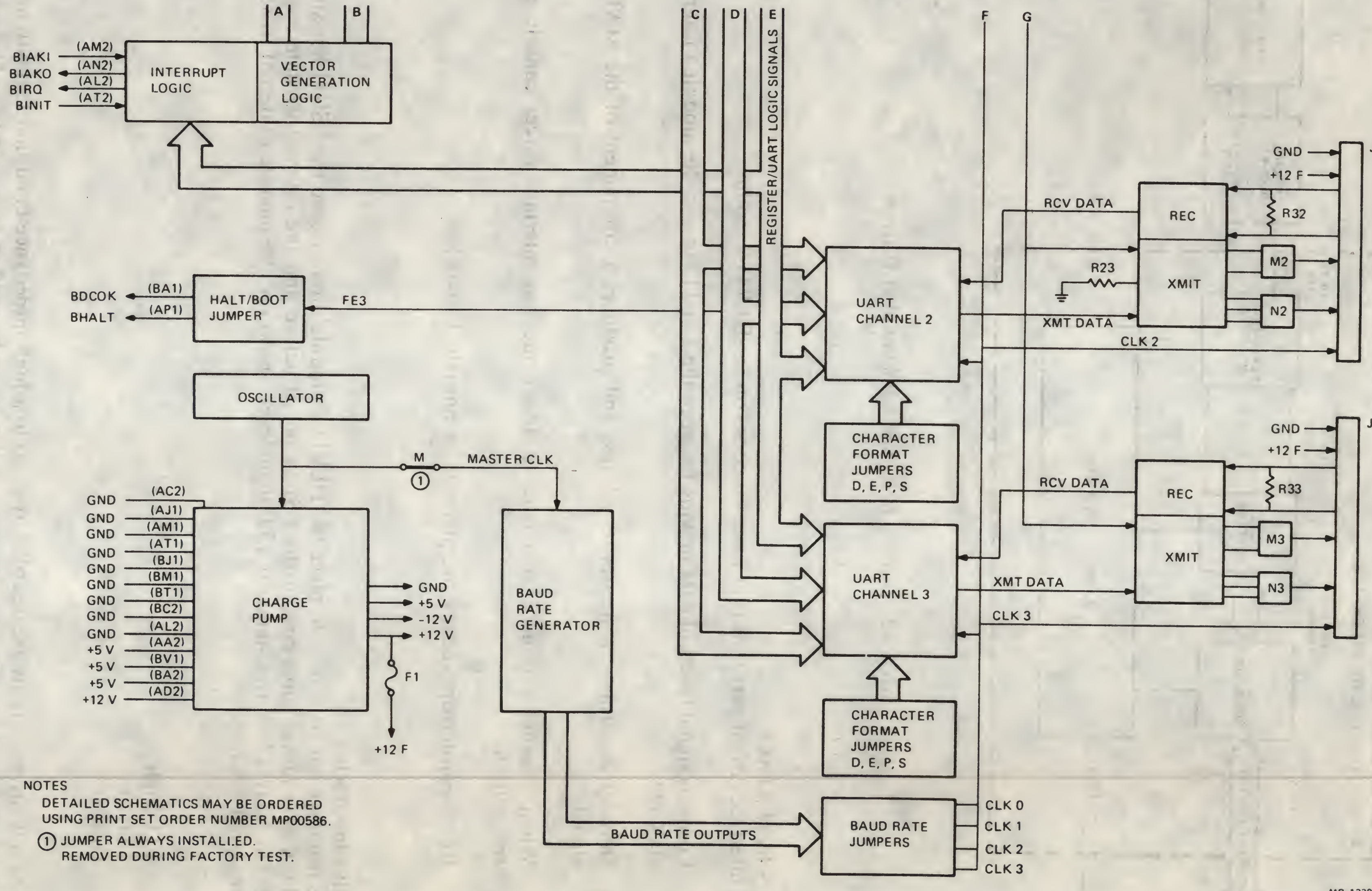


Figure 4-1 DLV11-J Block Diagram (Sheet 2 of 2)

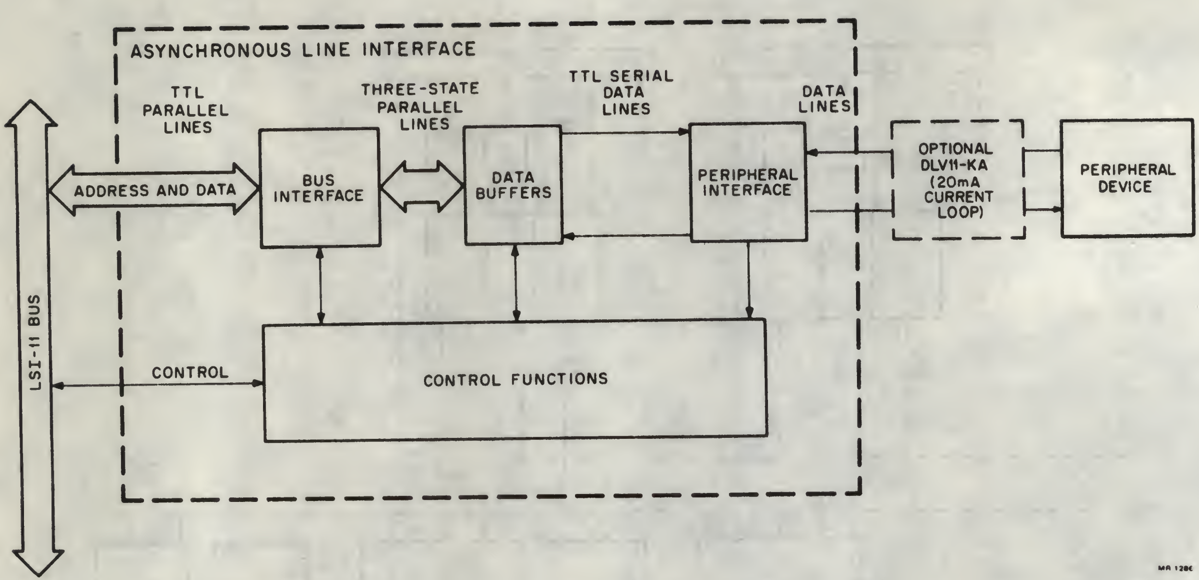


Figure 4-2 DLV11-J Data Flow, Simplified Block Diagram

4.3 BUS INTERFACE

The bus interface circuit performs four basic functions on the DLV11-J module.

1. Converts signal levels of data moving between the LSI-11 bus and the module's internal tri-state bus.
2. Decodes a portion of the device address and produces a component of the MATCH H signal.
3. When channel 3 is used as a console device the bus interface forces console address recognition.
4. Receives interrupt vectors and places them onto the LSI-11 bus.

4.3.1 Bus Interfacing

The bus interface circuit is used to place the DLV11-J module directly onto the LSI-11 bus structure. This allows data movement between the LSI-11 bus structure and the internal tri-state bus of the module. The LSI-11 bus uses standard TTL logic levels; however, the module's internal tri-state bus has three signal conditions:

TTL high
TTL low
Disabled.

When the bus driver outputs are disabled, they go to a high impedance condition that will not affect other devices connected to the bus. This permits the bus to be used in both directions by high-speed, low-power devices.

4.3.2 Address Comparison

The bus interface circuit monitors the LSI-11 data/address bus lines (BDAL) 0–15 during module operation (see Figure 4-3). It inverts these signals and places them on the appropriate internal tri-state buses DA 0–7 (data bus) and DA 12–15 (error bus) of the module. If the information on the BDAL lines is the address of a location in the upper 4K of addressing space; i.e., in the I/O page, the processor asserts the BBS7 L (Bank 7 Select) signal line. The signal enables the device address match function within the interface to compare the LSI-11 bus lines (BDAL 6–7) and the user-configured module base device resister address (wirewrap jumpers A6–7). If the addresses agree, the bus interface produces a component of the MATCH H signal required by the address latch (the remaining portion of MATCH H is discussed in Paragraph 4.5).

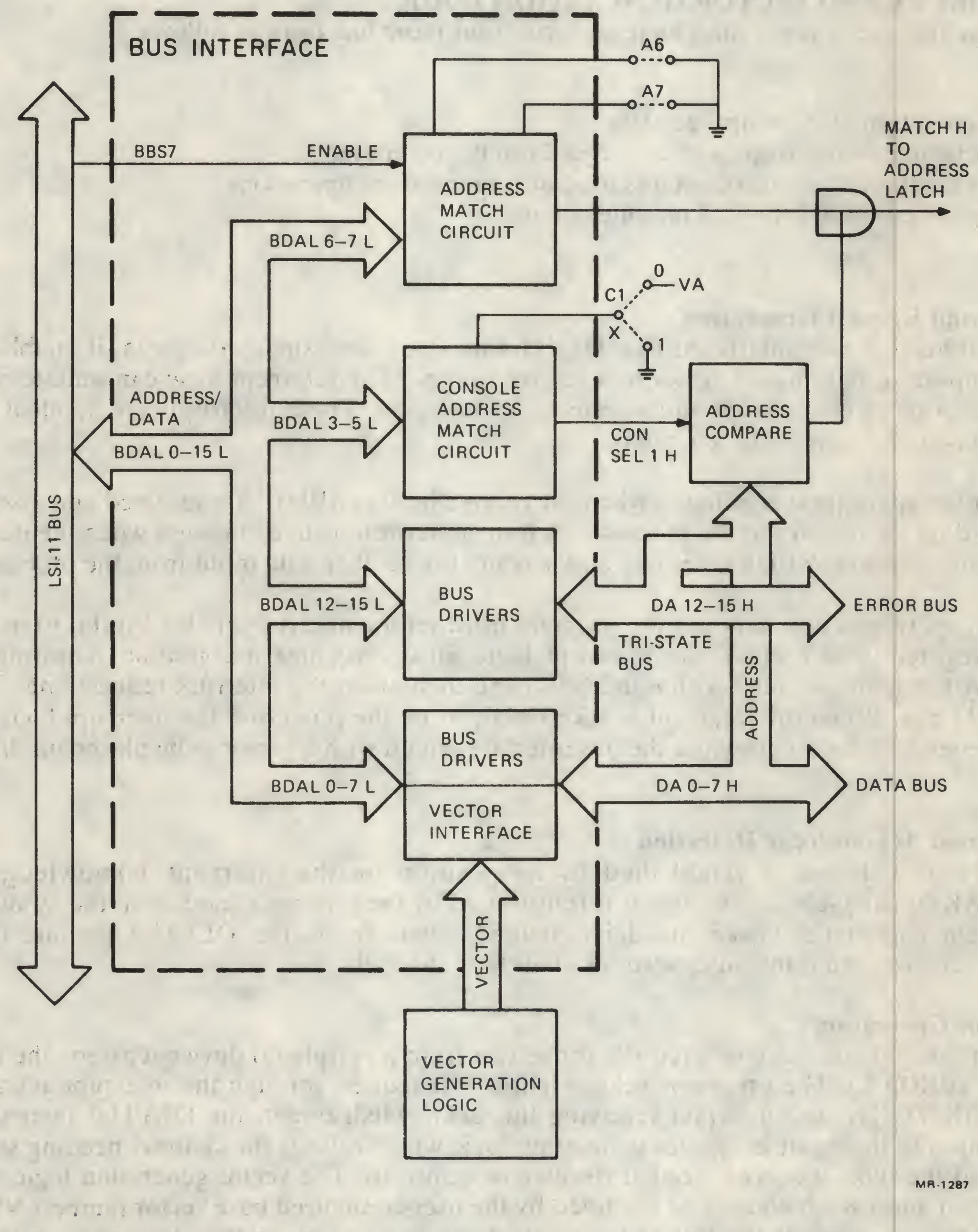


Figure 4-3 Bus Interface Signal Flow

4.3.3 Channel 3 Console Device Addressing

If channel 3 has been selected as a console device interface (jumpers C1 and C2 installed between wirewrap posts X and 1), the bus interface performs a match operation between the LSI-11 bus lines (BDAL 3-5) and an internal address. The internal address is enabled by the console select jumper C1. If these addresses agree, a CON SEL 1 H signal is produced for the address-compare circuit, causing console address recognition.

4.3.4 Vector Transmission

When the interrupt request function is enabled by the program, the bus interface circuit can place one of two vectors associated with each channel onto the BDAL bus lines. This vector is determined by the vector generation logic under control of the interrupt logic.

4.4 INTERRUPT AND VECTOR GENERATION LOGIC

The interrupt and vector generation logic performs four basic functions as follows.

1. Generation of interrupt requests
2. Detection of interrupt acknowledges from the computer
3. Generation of modified vectors used during interrupt operations
4. Initialization of DLV11-J module circuits

4.4.1 Interrupt Request Generation

When a peripheral device interfaced to a DLV11-J needs service, the module can, if enabled, interrupt the computer program and vector to a service routine. The interrupt logic can initiate two types of interrupts: a receiver interrupt and a transmitter interrupt. These interrupts are handled through separate receiver and transmitter channels.

A receiver interrupt request is initiated when the receive buffer (RBUF) has received and assembled a character of data for transfer to the processor. A transmitter interrupt is initiated when the transmitter buffer's holding register (XBUF) is empty and is ready for another data input from the processor.

For an interrupt transaction to occur, the program must set the interrupt enable bit (bit 6) in the control/status register (CSR). Next, the interrupt logic must recognize a condition requiring service (indicated by the setting of bit 7 within the CSR) and then assert the interrupt request line (BIRQ L) on the LSI-11 bus. When the interrupt is acknowledged by the processor, the interrupt logic enables the vector generation logic to provide the bus interface circuit with a vector to be placed on the LSI-11 bus.

4.4.2 Interrupt Acknowledge Detection

The priority of a device is established by its position on the interrupt acknowledge signal (BIAKI/BIAKO) daisy-chain. The signal is transmitted by the processor module to the modules held on the system backplane. When the daisy-chained signal enters the DLV11-J module it travels through the receiver and transmitter sections of all four channels.

4.4.3 Vector Generation

When the interrupt logic receives a request for service from a peripheral device it asserts the interrupt request line (BIRQ L). The processor acknowledges this request through the interrupt acknowledge (BIAKI/BAIKO) daisy-chain. Upon receiving this acknowledgement, the DLV11-J interrupt logic creates an input to the module's vector generation logic which reflects the channel needing service (0, 1, 2 or 3) and the type of service needed (receive or transmit). The vector generation logic creates a vector function address which may be modified by the user-configured base vector jumpers V5-7. This modified address is output to the LSI-11 bus by the bus interface circuit, thus causing the processor to jump to the proper peripheral device service routine.

4.4.4 Board Initialization

The interrupt logic is used to initialize the DLV11-J module. During a system power-up sequence a BINIT L signal is asserted on the LSI-11 bus and is converted by the DLV11-J's interrupt logic to the INITO H signal. This signal is distributed on the module to initialize the four UARTs and the interrupt status registers (held within the interrupt logic).

4.5 ADDRESS COMPARE

The address compare circuit tests the user-configured wirewrap board address (A5, A8–12) against the LSI-11 bus input (BDAL 5, BDAL 8–12) to create a component of the MATCH H signal. The MATCH H signal is required by the address latch during module operation. (The address latch receives the remaining component of MATCH H from the bus interface circuit discussed in Paragraph 4.3.2.)

Bus lines BDAL 8–11 are received directly by the address compare circuit to be tested against the predetermined conditions created on base address wirewraps A8–11 (as shown in Figure 4-4). In addition, the address compare logic receives the bus input BDAL 5 and 12 indirectly through the bus interface circuit (which merely inverts the signals and places them on the internal tri-state bus). The BDAL 5 and 12 inputs are tested by the address compare circuit against the conditions created by the base device register address jumpers A5 and A12. If all the address compare inputs match, the MATCH H signal is asserted. (A summary of the board address decoding is shown in Figure 4-5.)

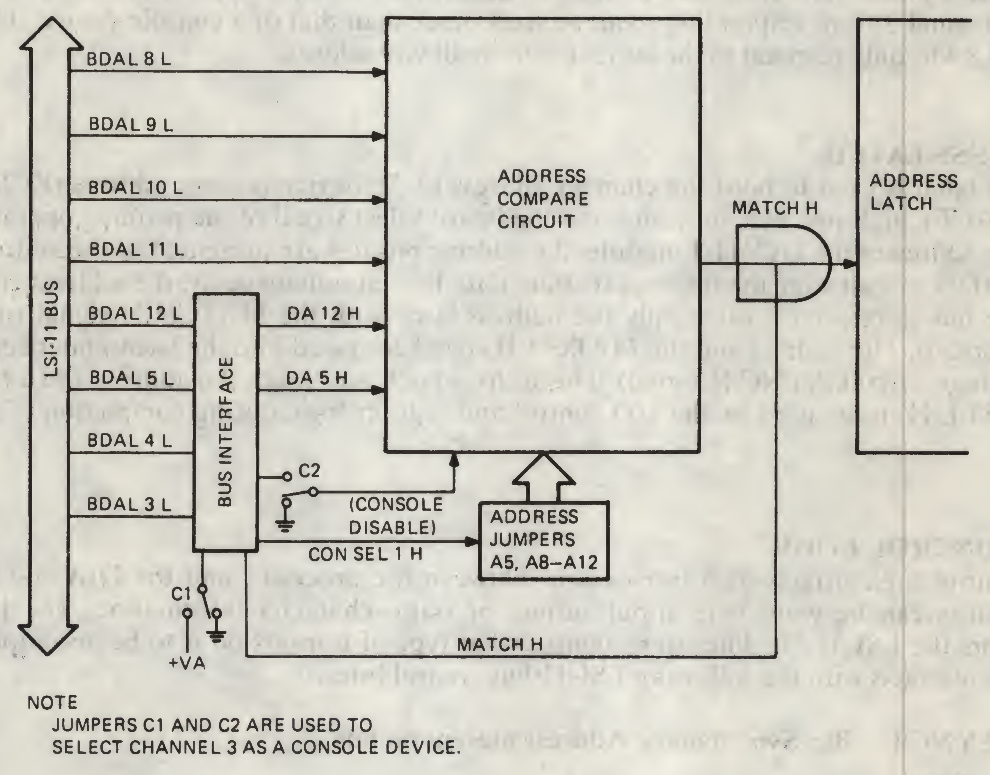


Figure 4-4 Address Compare Circuit Block Diagram

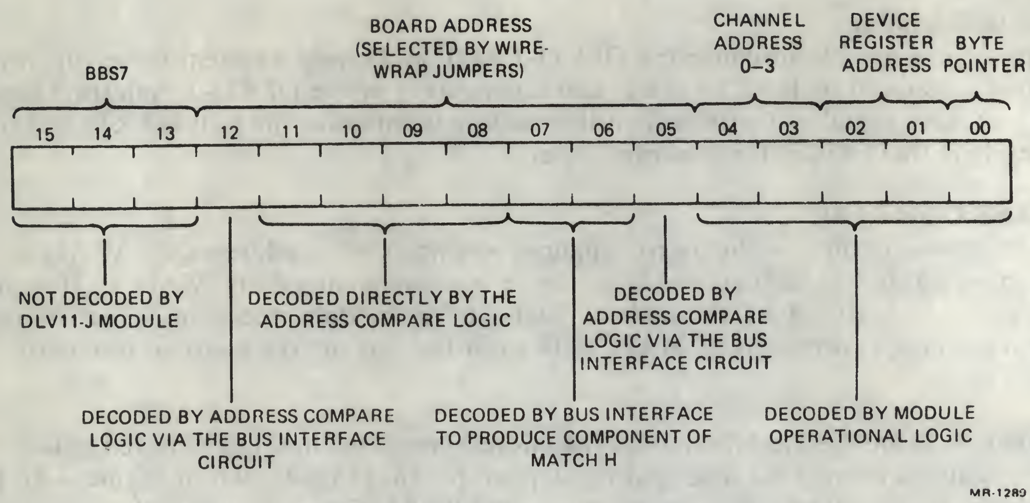


Figure 4-5 Summary of Board Address Decoding

When channel 3 is configured as a console device, the bus interface circuit supplies the address compare logic with two additional signals: CON SEL 1 H and channel 3 address disable. CON SEL 1 H is created by the bus interface when comparing an internally held address with bus lines BDAL 3–5. When a match is achieved, the CON SEL 1 H signal is transmitted to the address compare logic to force an address match. The channel 3 address disable (provided by console select jumper C2) is used to prevent channel 3 from responding to an address other than that of a console device. This ensures that channel 3 will only respond to the correct console device address.

4.6 ADDRESS LATCH

The address latch is used to hold the channel address (0–3), device register address (RCSR, RBUF, XCSR or XBUF), high-low byte indicator and the board select signal of the pending operation. When the program addresses the DLV11-J module, the address bits 0–4 are presented to the address latch by the bus interface circuit over the internal tri-state data bus. Simultaneously, the address compare circuit and the bus interface circuit supply the address latch with the MATCH H signal (if the board address is correct). The address and the MATCH H signal are gated into the latch under control of the I/O control logic circuit (SYNC H signal). The address latch now holds the address and a board select signal (BD SEL H) to be used by the I/O control and register logic during completion of the desired operation.

4.7 I/O CONTROL LOGIC

The I/O control logic directs data transactions between the processor and the DLV11-J module. A data transaction can be word-byte, input-output, or status-character information. The I/O control logic monitors the LSI-11 bus lines to recognize what type of transaction is to be accomplished. The control logic interacts with the following LSI-11 bus control lines.

BSYNC L – Bus Sync signal – Address present on bus

BDIN L – Bus Data In – Ready to accept data or interrupt operation occurring

BDOUT L – Bus Data Out – Data output valid

BRPLY L – Reply from Module – Data output or input complete

The control logic uses this information to operate the four device registers of each channel by creating BD DIN/BD DOUT module gating signals. The register names and functions held within each channel are as follows.

Receiver Control/Status Register	RCSR
Transmitter Control/Status Register	XCSR
Receiver Buffer	RBUF
Transmitter Buffer	XBUF

The I/O control logic operates during three types of data transfers:

Interrupt operations
Input operations
Output operations.

Interrupt operations occur when the interrupt logic of the DLV11-J creates an interrupt request (BIRQ L) signal. The processor acknowledges the interrupt request via the BIAKI/BIAKO daisy-chain, thus causing the module's interrupt logic to initiate a vector generation. Upon assertion of BIAKI L, the DLV11-J interface places the vector onto the LSI-11 bus where it is read by the computer. The I/O control logic senses that the vector has been produced by the activation of the VECTOR 1 H signal and in turn produces the BRPLY L signal. BRPLY assertion indicates the end of the interrupt vector transfer, thereby causing the negation of the LSI-11 bus control signals.

4.7.2 Input Operation

When the computer program reads data from the DLV11-J module (DATI bus cycle), the module's address is placed onto the LSI-11 bus lines BDAL 0–15 and the BBS7 L signal line is asserted. The BSYNC L signal line of the computer latches this address into the module where it is decoded to produce a BD SEL H signal. The BD SEL H signal is presented to the I/O control logic, indicating a proper address was received. Subsequently the address is removed from the bus, BBS7 L is negated and the processor asserts the BDIN L signal. The I/O control logic on the reception of the BDIN L signal gates the contents of the desired register to the LSI-11 bus (via the bus interface circuit) and asserts BRPLY L. The computer reads the data and negates the BDIN L signal, indicating the end of the data transfer. The BRPLY L and BSYNC L signals are deactivated to end the bus cycle.

4.7.3 Output Operations

When the computer writes a word or byte out to the interface module (DATO or DATOB bus cycle), the module's address is placed onto the BDAL 0–15 LSI-11 bus lines and BBS7 L is asserted. The BSYNC L signal of the bus latches the address into the module where it is decoded to produce a BD SEL H signal for the I/O control logic. The BD SEL H signal indicates the proper board address was received and module operation may continue. The address is removed from the LSI-11 bus, BBS7 L is negated and the data to be transferred is placed onto the bus. The computer asserts BDOUT L, causing the I/O control logic to gate the data to the proper device register. BRPLY L is issued by the I/O control logic, indicating that the data transfer has been completed. The computer removes the data from the bus and negates BDOUT L. The module negates BRPLY L, and the computer negates BSYNC L, terminating the bus cycle.

4.8 REGISTER LOGIC

The DLV11-J has two control/status registers (CSR) for each of its four channels – the receiver control/status register (RCSR) and the transmitter control/status register (XCSR). The registers consist of latches, data selectors and gating circuitry which operate under the direction of the I/O control logic on the module. Input I/O control logic enables the registers to either latch in control bits or gate out status bits during operation.

Each of the registers can be individually addressed by the processor when using the proper unique device register address. The register's address is an offset of the base device address configured on the module. However, when channel 3 is selected as a console device, standard console addresses are used by the channel.

When status bits are to be read by the computer, the input data transfer (DATI) operation places the device register address onto the LSI-11 bus. The module decodes the address and the content of the register is gated through the module's bus interface circuit to the LSI-11 bus. (See Figure 4-6.)

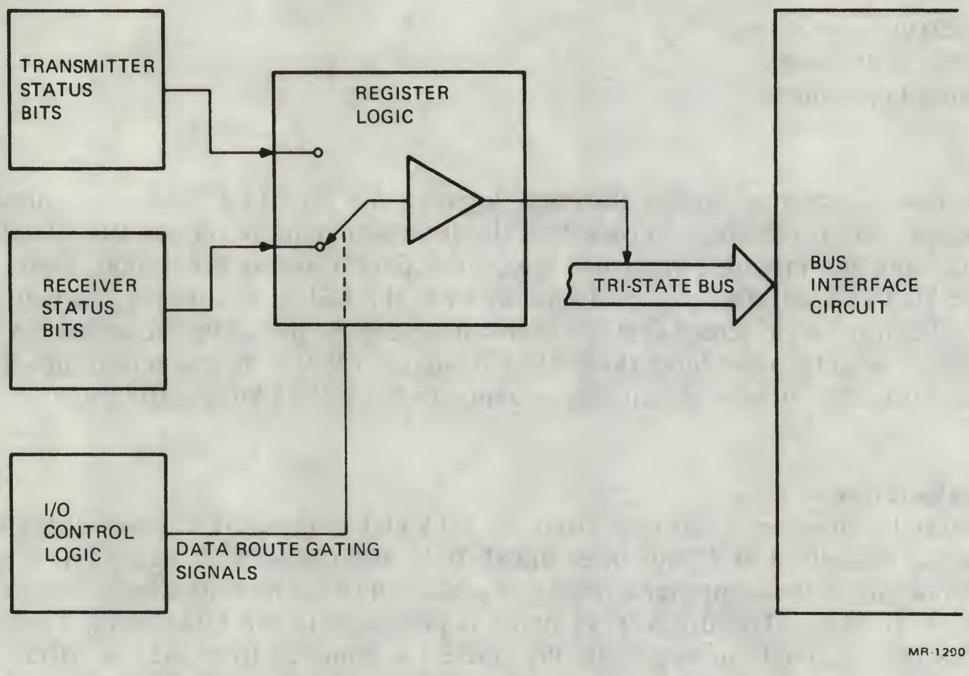


Figure 4-6 Control/Status Register During DATI

Control information may be written out of the computer with the use of an output data transfer (DATO or DATOB) operation. The address of the device register to be loaded is placed onto the LSI-11 bus where it is read by the DLV11-J. The address is decoded and the proper device register enabled to accept the control information. When the information is placed onto the LSI-11 bus, the I/O control logic of the module gates it through the bus interface circuit to the enabled CSR. (See Figure 4-7.)

4.8.1 CSR Data Flow

The receiver control/status register (RCSR) uses three bits during operation: the receiver done bit (bit 7), receiver interrupt enable bit (bit 6) and reader enable bit (bit 0). The receiver done bit is set by the receiver buffer when a character has been assembled and is ready for input to the processor. This bit works in conjunction with the receiver interrupt enable bit to initiate interrupt requests. The receiver interrupt enable bit is set by the program to allow interrupt requests to occur. Interrupt requests are generated whenever both the interrupt enable bit (bit 6) and the receiver done bit (bit 7) are set.

The reader enable bit (bit 0) is used to advance a paper tape reader one character, thus allowing data to be input into the system. This bit is functional only when the DLV11-KA option is used with the DLV11-J module. The reader enable bit is program-controlled and is the only bit of the RCSR which cannot be read; it is a write only bit. The RCSR operational data flow is pictured in Figure 4-8.

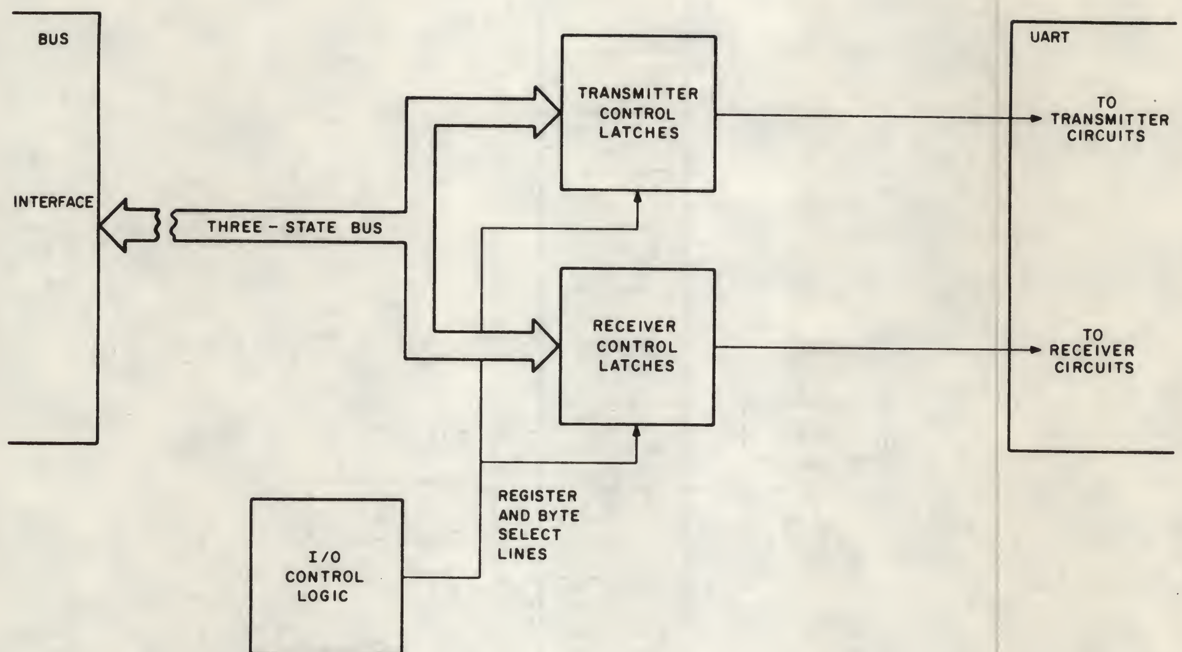


Figure 4-7 Control/Status Register During DATO or DATOB

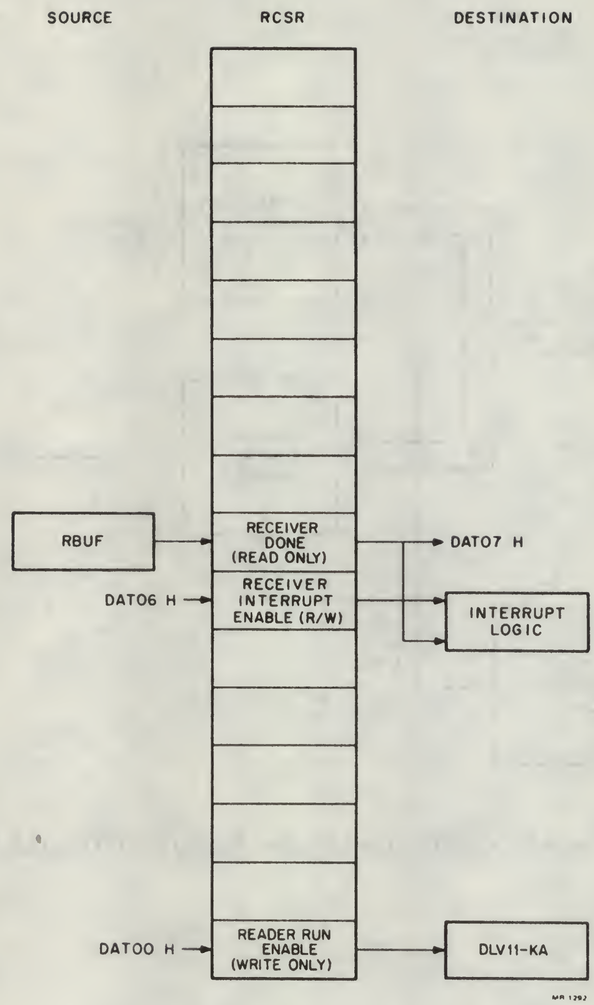


Figure 4-8 DLV11-J RCSR Data Flow

The transmit control/status register (XCSR) only uses three bits during operation: the transmit ready bit (bit 7), transmit interrupt enable bit (bit 6) and transmit break bit (bit 0). The transmit ready bit is set by the transmit buffer when it is empty and can accept another character for transmission. The transmit ready bit works with the transmit interrupt enable bit to generate transmitter interrupts. Transmit interrupt enable (bit 6) is set by the program to allow interrupt requests to be generated. Transmitter interrupts may occur when both the transmit ready bit and transmit interrupt enable bit are set.

Transmit break bit (bit 0) is set or reset under program control. When set, the module will transmit a constant space level; however, both the receiver done and transmit interrupt enable remain fully operational. The XCSR data flow is shown in Figure 4-9.

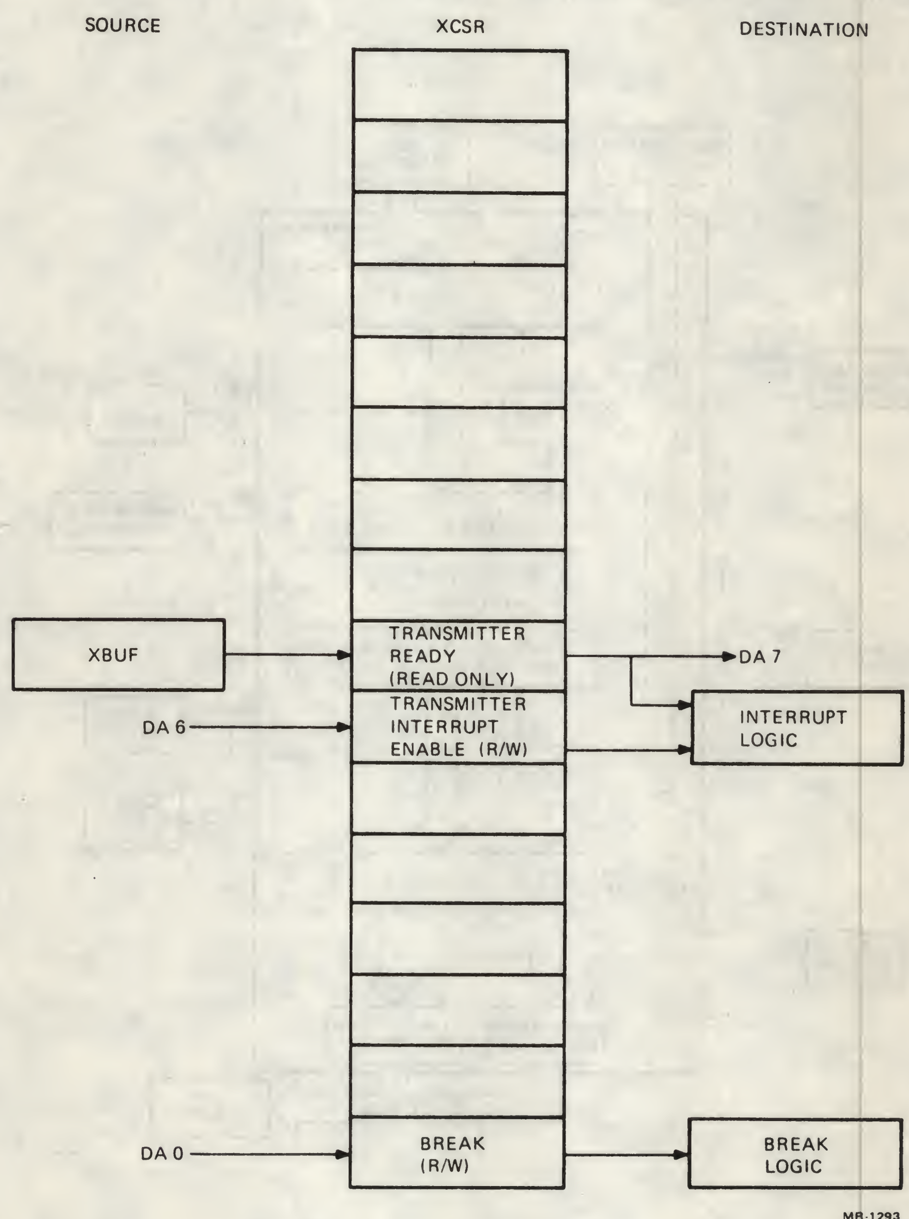


Figure 4-9 DLV11-J XCSR Data Flow

4.9 UNIVERSAL ASYNCHRONOUS RECEIVE TRANSMITTER (UART) OPERATION

4.9.1 General

The DLV11-J module is equipped with four universal asynchronous receiver/transmitter (UART) chips, one per channel. These chips are capable of serial data transfers with the peripheral device interface and parallel data transfers with the module's internal bus (and thus, with the processor). Both the receive and transmit data buffers of a channel are held within a single UART chip. The receiver section performs the receiver buffer (RBUF) function, accepting asynchronous serial binary data characters, converting them to a parallel format, and placing them onto the module's internal tri-state bus. The transmitter section performs the transmit buffer (XBUF) function, accepting parallel data from the module's internal bus and converting it to a serial data format for the peripheral device interface. The baud rate and character format used during these data transfers is user-selectable when configuring the module (see Chapter 2 for details on board configuration) prior to installation. A simplified block diagram of the UART is shown in Figure 4-10.

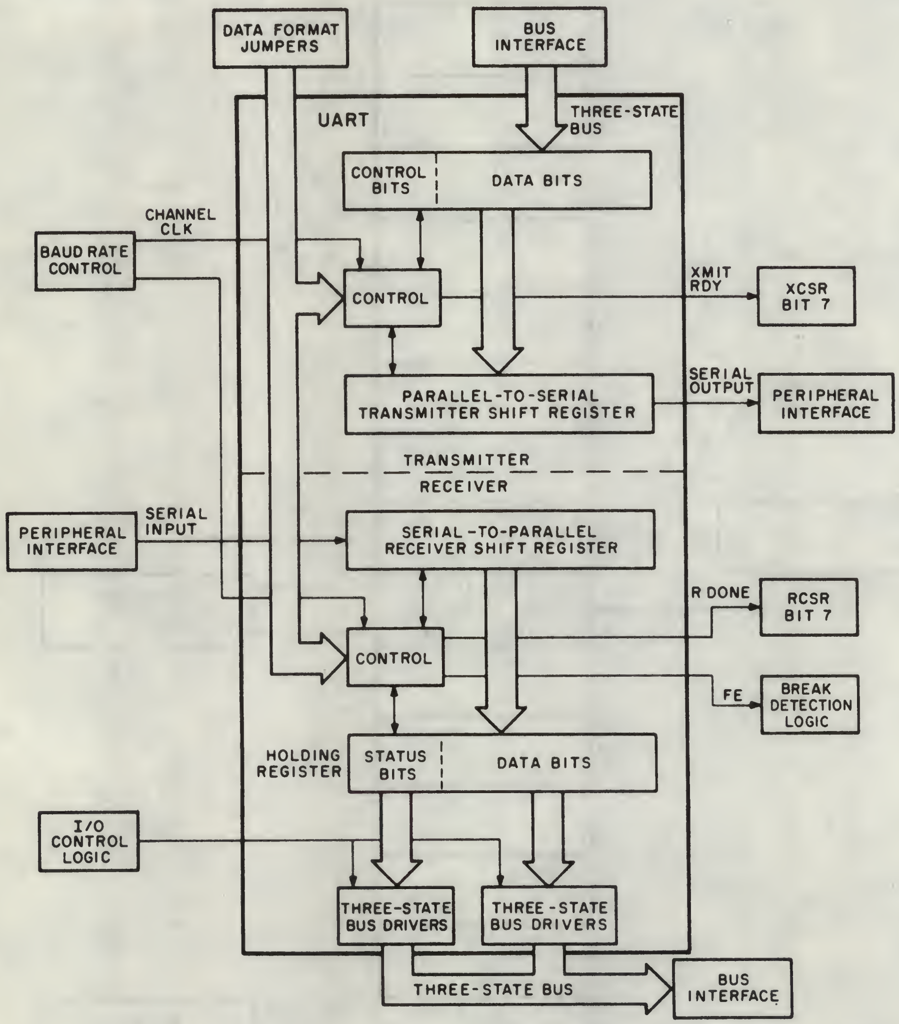


Figure 4-10 UART Signal Flow (Typical for All Channels)

4.9.2 Receiver Operation

The UART receiver consists of two data buffers (one serial, one parallel) and their controlling logic which provide the channel with all receive buffer functions. The receiver section accepts asynchronous serial binary characters, converts them to parallel format and places them onto the internal tri-state bus of the module.

Serial data entering the module from the peripheral device is converted to TTL signal levels by the peripheral interface circuit and applied to the UART's receiver section. The UART samples the serial input data line at 16 times the data bit rate and will sense a continuous marking state when idle. When a START bit arrives, the UART detects a mark-to-space transition and begins loading the character into the receiver shift register. The character is shifted to place the least significant bit in the lowest bit position of the register.

When the UART receives the first STOP bit, it transfers the data in parallel from the receiver shift register to the parallel holding register (see Figure 4-11), removing all START, STOP or parity bits from the transmission. At this time, the data and error bits become valid for gating onto the module's tri-state bus and the receiver asserts receiver done (bit 7 of the RCSR). If the receiver interrupt enable bit (bit 6) is set, an interrupt request is initiated. The computer then has one full character period to service the interrupt before the next character is moved into the holding register. During this time the next character (if available) is being assembled in the receiver shift register. After the DATI (data input) sequence has taken the data, the I/O control logic resets the receiver done bit (bit 7) of the RCSR. If the computer program does not take the data within the character time allotted the RCVR done does not get reset, thus causing an error condition.

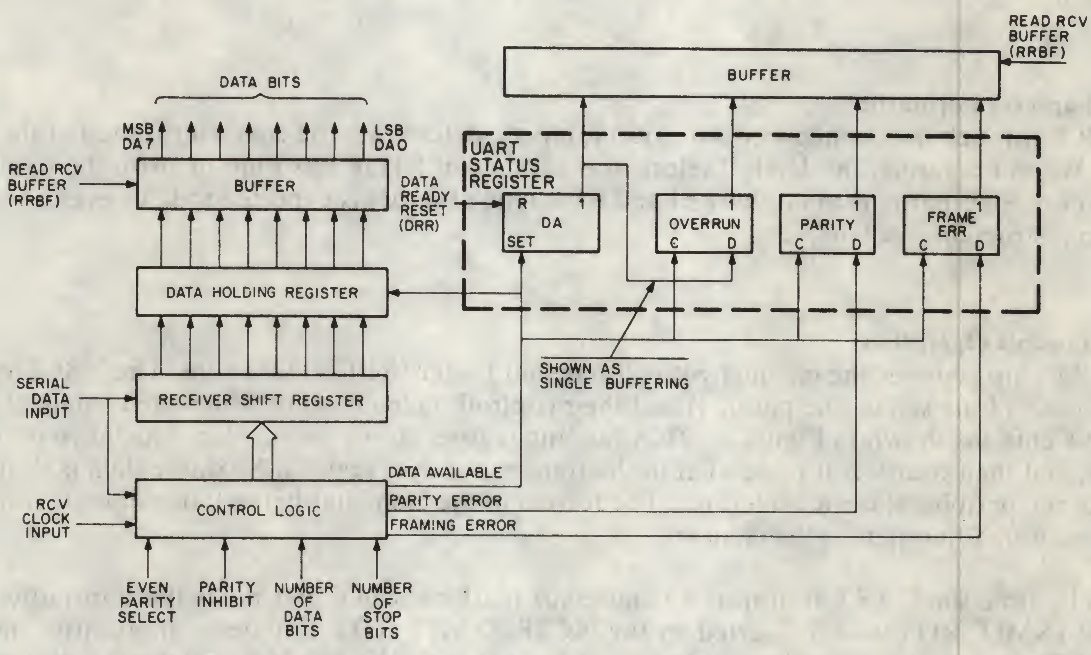


Figure 4-11 UART Receiver Block Diagram

4.9.2.1 Error Detection

The DLV11-J uses the UART to sense three types of communication errors:

FE Framing errors
OE Overrun errors
PE Parity errors.

4.9.2.2 Framing Errors (FE) - A framing error is produced when the UART does not receive a valid STOP bit(s). A valid STOP bit is received when the line is found marking at the correct bit time. If the line is spacing when the UART tests for a STOP bit(s) the framing error flag will be set.

4.9.2.3 Overrun Error (OE) - When the receiver done bit (bit 7) is set, the computer is given one full character time to read the receive buffer. If the program does not read the data before the next character is completely assembled within the holding register, the UART will set the data overrun flag. The setting of the flag indicates the first character was lost.

4.9.2.4 Parity Error (PE) - If the channel is jumpered for parity checking (P jumper set between wirewraps X and 0), the UART will check the MARKs received in the data and parity bits of each character. If the UART finds an even count and even parity has been selected (E jumper installed between wirewraps X and 1) or if an odd count is found and odd parity has been selected (E jumper installed between wirewraps X and 0), the flag is left cleared. If any other condition occurs the UART will set the parity bit indicating a data transmission error.

4.9.2.5 Error Flag - Any error condition (OE, PE, or FE) found by the UART will set the ERR flag bit 15. This flag indicates that some type of transmission error has occurred.

These error bits do not initiate interrupt requests, but they are available for the programmer in the receive buffer.

4.9.3 Character Formatting

The UART, through user-configured wirewrap jumpers, determines the character format of the transmission. When operating, the UART selects the number of STOP bits (one or two), the number of data bits (7 or 8), if parity is to be checked and what type of parity is expected (odd or even). For configuration instructions see Chapter 2.

4.9.4 Transmit Operation

The UART chip supplies the channel with all transmit buffer (XBUF) functions. The XBUF consists of two registers (one serial, one parallel) and their controlling logic, all of which are contained within the UART chip (as shown in Figure 4-12). A holding register stores the parallel data taken off the tristate bus, and then transfers it in parallel to the transmitter shift register. Next, the data is shifted out serially to the peripheral device interface. The format of the character being transmitted is controlled by the data format jumpers of the channel.

During idle time the UART transmits a continuous marking signal and holds the transmitter ready status bit (XMIT RDY bit 7) asserted in the XCSR; XMIT RDY initiates a transmitter interrupt request if the transmitter interrupt enable bit (bit 6) is set in the XCSR. If the interrupt function is not enabled, the UART transmitter remains idle until the program requires it.

When the program has data to transmit to a peripheral device, it uses a DATO (data output) or DATOB (data output byte) sequence to load the XBUF register. The bus interface receives the data to be transmitted from the LSI-11 bus lines (BDAL 0-7 L) and transfers it to the (DA 0-7 H) tri-state bus of the module. The I/O control logic gates this data into the holding register of the XBUF (held within the UART). When the data enters the holding register, the UART negates XMIT RDY. The character is then transferred to the transmitter shift register to be shifted serially out of the XBUF and into the peripheral interface circuitry.

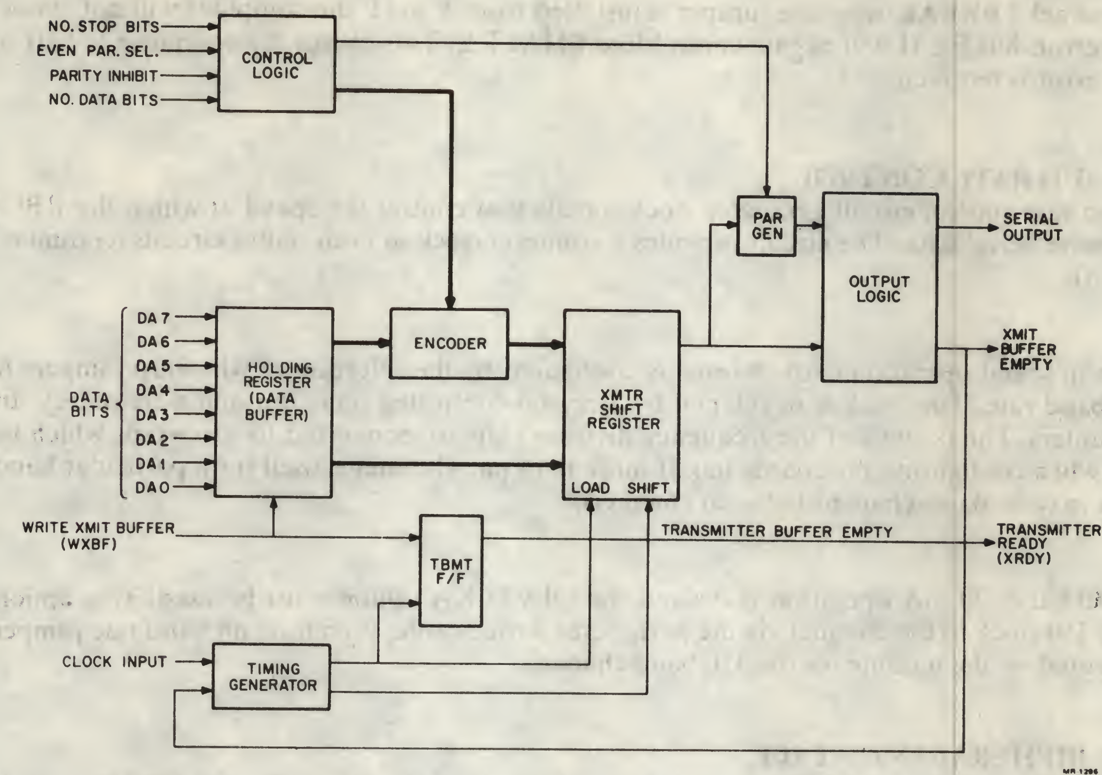


Figure 4-12 UART Transmitter Block Diagram

XMIT RDY is asserted as soon as a character is transferred from the holding register to the transmitter shift register, thereby indicating that the holding register is empty. The next character may be loaded immediately, even while the first character is still being serially shifted out of the transmitter shift register. Hence, if the holding register and transmitter shift register are both empty, the computer can parallel-transfer a 2-character pair into the XBUF in less time than it takes for a single character to be serially transmitted to the peripheral device. This advantage of double-buffering applies only to the first two characters; that is, if a series of characters is being transmitted, each character after the second must wait a serial character period for the XBUF to become ready again. The actual time depends on the baud rate of the channel.

4.10 BREAK LOGIC

During normal operation, the UART checks each received character for the proper number of STOP bits. It does this by testing for a marking condition at the appropriate bit time. If the UART finds a spacing condition instead, it sets the framing error flag (FE). The BREAK signal is a continuous spacing condition, and is interpreted by the UART as a data character that is missing its STOP bit(s). The UART, therefore, responds to the BREAK signal by asserting FE H. If the channel 3 BREAK response jumper is installed from X to B, FE H will negate control line BDCOK H; BDCOK H indicates to the processor that dc power is "OK." When FE H negates this signal, it causes the computer to jump to location 173000 (normally ROM boot).

CAUTION

If the LSI-11 is using MOS memory with processor refresh, data may be lost when BDCOK H is negated during memory refresh because this action interrupts the memory refresh cycle. If the channel 3 break response jumper is not installed, the module will not take action.

If the channel 3 BREAK response jumper is installed from X to H, the computer will not "boot" on a framing error, but FE H will negate control line BHALT L. This causes the computer to halt when a framing error is received.

4.11 BAUD RATE CONTROL

The baud rate control circuit generates clock signals that control the speed at which the RBUF and XBUF move serial data. The circuit provides a common clock to both buffer circuits (common speed operation).

In common speed operation each channel is configured by the selection of wirewrap jumpers for the desired baud rate. The clock is developed by a crystal-controlled oscillator and a frequency division chip (counter). The outputs of the frequency division chip are connected to wirewraps which may be selected when configuring the channel(s). If more than one channel is used for a particular baud rate, the clock may be daisy-chained between channels.

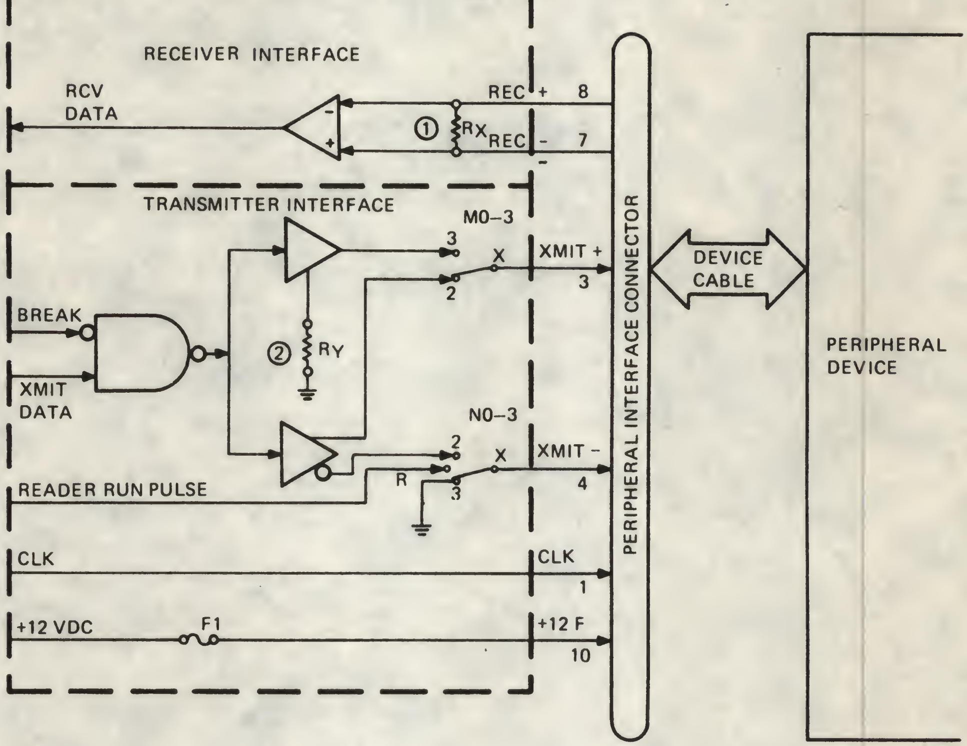
When 110 baud, 20 mA operation is desired the DLV11-KA option must be used. This option provides the 110 clock to the channel via the peripheral device cable; therefore, no baud rate jumper may be configured on the module for the 110 baud channel.

4.12 PERIPHERAL INTERFACE

Each SLU channel of the DLV11-J module can be independently configured for line signal compatibility with EIA RS-232C, RS-423, RS-422 and 20 mA current loop operation (see Figure 4-13). Each of the four interfaces may be configured to support 20 mA current loop devices with the addition of the DLV11-KA option. When installed, the peripheral interface supplies all power supply voltages needed by this option. If the 20 mA device contains a paper tape reader that can be program-controlled (such as a DEC-modified LT-33 Teletype) the interface can be configured to supply the needed reader enable pulses. For specific instructions on peripheral interface configurations see Chapter 2.

4.13 DC-TO-DC POWER CONVERTER

The power converter produces -12 Vdc from the LSI-11 power supply voltage of +12 Vdc and +5 Vdc. The power converter circuit consists of a crystal-controlled oscillator which drives a charge pump. The charge pump during operation supplies -12 Vdc to the EIA driver chips.



NOTES

① R_X IS INSTALLED WHEN CHANNEL IS CONFIGURED FOR EIA RS-422 OPERATION (100 Ω, 1/4 W NON-WIRE WOUND)
R30 - CHANNEL 0
R31 - CHANNEL 1
R32 - CHANNEL 2
R33 - CHANNEL 3

② R_Y IS CHOSEN FOR PROPER SLEW RATE WHEN CHANNEL IS CONFIGURED FOR EIA RS-232C/RS-423 OPERATION
R10 SETS SLEW RATE FOR CHANNELS 0 AND 1
R23 SETS SLEW RATE FOR CHANNELS 2 AND 3

MR 1297

Figure 4-13 Typical Peripheral Interface

APPENDIX A
DLV11-KA USER'S GUIDE

NOTE

The DLV11-KA 20 mA option is not available at this time. Option information will be contained in the next revision of this manual.

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